MAX3760 Output Model

SPICE I/O Macromodels aid in understanding signal integrity issues in electronic systems. Most of Maxim's High Frequency/Fiber Communication ICs utilize input and output (I/O) circuits with Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) formats to transfer data into and out of an IC. These models are based on simplified circuit expressions that may include replacement of active circuit elements with ideal controlled voltage and current sources. As such, simulation with macromodels should be treated as 'typical' performance and not relied upon as final proof-of-design. Use of macromodel descriptions is not a substitute for worst-case design analysis, nor for testing real circuits over temperature, supply, and other operating limits.

The output format is provided as ASCII text netlists suitable for generic SPICE. This format is compatible with most versions of SPICE such as PSPICE and HSPICE. Additional information is found in HFAN 6.1 *Input/Output Models for Maxim Fiber Component*s.

To extract the circuit netlists using the Adobe Acrobat Reader follow these instructions. Select the "Text Select Tool" by clicking the left mouse button on this icon of the menu bar (a capital T with a small dashed box to the lower right). Highlight the desired netlist text with the cursor. Use the copy command from the edit menu to capture the selected lines. Then paste the selected lines into a text file editor and save the file with an extension compatible with the simulator.

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I/O Models for the MAX3760

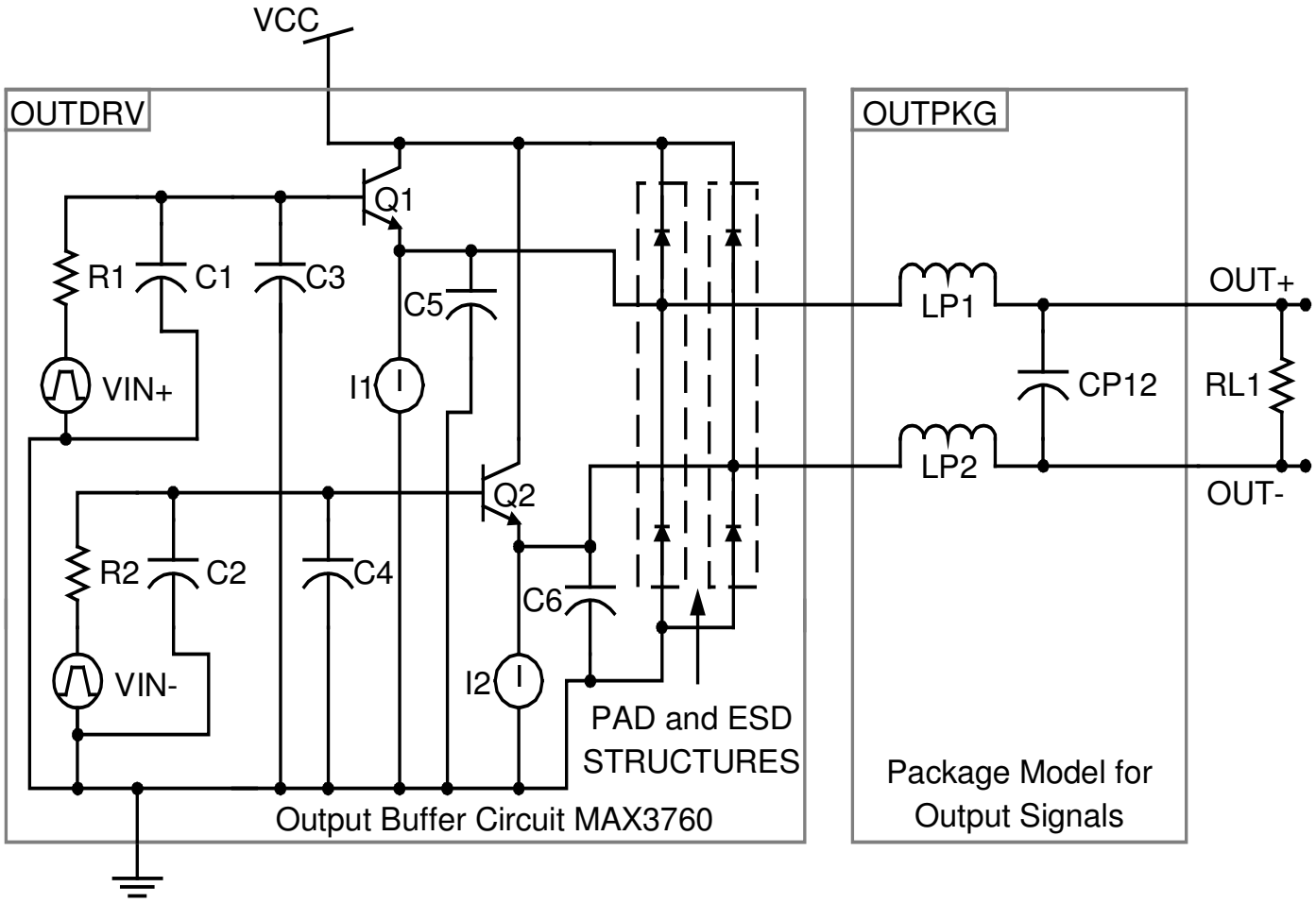

Figure 1. Output model for signal OUT of the MAX3760.

Notes:

The schematics on the previous page represent the output stage of the Maxim MAX3760 622Mbps Transimpedance Preamplifier. The output circuit shown is for the signal outputs (OUT+, OUT-). However the models are given in generic SPICE, which only accepts node names as numbers. As discussed in the application note, the output signals are described as (2001, 2002). This model is only valid at 25°C. The bias current for the output circuitry is modeled by an ideal current source. This model is compensated for variations in VCC, so VCC equal to 5V should be used. ESD and PAD structures have been modeled.

The package model has had all of the parasitic components calculated. If the die form of the part is used, then it is simple to remove the OUTPKG subcircuit from the netlist.

The Output Stage: The output stage of the MAX3760 is shown as the sub-circuit "OUTDRV".

The OUTDRV Sub-circuit: The outdrv sub-circuit is a simplified version of the output stage used by the MAX3760 Transimpedance Preamplifier. The output stage is terminated differentially with 100Ω. The output waveform is configured to be at a differential voltage of 550mV peak to peak. The output common mode voltage has been set to 3V. The output waveform has a frequency of 311Mhz. The netlist is given in SPICE 2G6 format in Appendix A.

Text File Format: This model is shipped in "pdf" format. Models and netlists can be copied to text format in the Acrobat Reader by holding the left mouse button on the "Text Select Tool." Then the user can "select" what netlist and/or subcircuit with the mouse. Then use the copy command from the "edit" menu to capture the selected lines. These lines can then be "pasted" into the user's text file.

Appendix A: Output Netlist

```
* 3760 Output Model
************************************************
.OPT ACCT NOMOD LIMPTS=10000
.TEMP 25
.OP
.TRAN 2P 10n
************************************************

* Voltage Source
VCC 101 0 5
* Differential Load Resistance
RL 2001 2002 100

************************************************
XOUTPKG 2001 2002 50 51 OUTPKG
XOUTDRV 50 51 101 OUTDRV
************************************************

************************************************
.SUBCKT OUTDRV 50 51 101

VINP 1  0 PULSE (3.664 4.02 0.04n 0.40n 0.40n 1.2n 3.21543n)
VINN 3  0 PULSE (4.02 3.664 0.04n 0.40n 0.40n 1.2n 3.21543n)

R1 2 1 50
R2 4 3 50

C1 2 0 5p
C2 4 0 5p
C3 2 0 15f
C4 4 0 15f
C5 50 0 38f
C6 51 0 38f

XQ1 101 2 50 0 H14E04
XQ2 101 4 51 0 H14E04

I1 50 0 3.4mA
I2 51 0 3.4mA

XD1 50 101 0 HDE113032
XD2  0  50 0 HDE113032
XD3 51 101 0 HDE113032
XD4  0  51 0 HDE113032
```

```
XP1 50 0 HPAD3
XP2 51 0 HPAD3

.ENDS OUTDRV
************************************************

************************************************
.SUBCKT OUTPKG 2001 2002 50 51

LP1   50 2001 5N
LP2   51 2002 5N
CP12 2001 2002 1p

.ENDS OUTPKG
************************************************

************************************************
* Transistor Model
.SUBCKT H14E04 1 2 3 21
CP1EPI 1 2 12.185F
CP1P2 12 3 19.634F
CTRENCH 1 20 15.307F
RBX 2 12 20.554 TC=2.663M
RCX 1 10 23.509 TC=2.354M,979.573N
RCI 10 11 1.237 TC=2.354M,979.573N
REX 13 3 2.795 TC=123.150U
RSUB 20 21 6.195K
QP 20 10 12 20 TXP OFF
QN 11 12 13 11 TX
.MODEL TX NPN( IS=3.326E-017 XTI=3 EG=1.140 BF=232.533 BR=20 XTB=450M
+   VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=126.546M
+   IKR=2.318M ISE=1.573E-020 ISC=2.022E-029 RB=20.554 RBM=15.416
+   IRB=20.223M CJE=107.672F MJE=490M VJE=940M FC=990M CJC=21.929F
+   MJC=470M VJC=850M TF=3.778P TR=19N XTF=1 VTF=1K ITF=59.621M PTF=5
+   KF=1.500F AF=1 )
.MODEL TXP PNP( IS=1.968E-018 CJE=21.929F MJE=470M VJE=850M CJC=21.582F
+   MJC=400M VJC=650M BF=10K BR=809.067U TF=1N FC=900M )
.ENDS H14E04
************************************************

************************************************
* ESD Diode Model
.SUBCKT HDE113032 1 2 21
CP1EPI 1 4 88.881F
QD 5 4 1 5 QESD
RS 4 2 2.531 TC=2.729M,1.896U
```

```
RSUB 5 21 2.936K
CTRENCH 2 5 22.961F
.MODEL QESD PNP( IS=1.181E-017 NF=1.050 BF=800M BR=600U CJE=155.018F
+   VJE=600M MJE=400M CJC=53.258F VJC=650M MJC=400M )
.ENDS HDE113032
************************************************

************************************************
* Pad Model
.SUBCKT HPAD3 1 3
CPAD 1 10 86.407F
REPI 10 20 149.204M TC=4.800M,5U
CTRENCH 21 20 79.795F
DS 21 20 DSUB
RS 3 21 369.115
.MODEL DSUB D( IS=98.719F CJO=555.750F M=400M VJ=650M )
.ENDS HPAD3
************************************************

.PROBE
.END
```