

## MAX3640 I/O Model

SPICE I/O Macromodels aid in understanding signal integrity issues in electronic systems. Most of Maxim's High Frequency/Fiber Communication ICs utilize input and output (I/O) circuits with Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) formats to transfer data into and out of an IC. These models are based on simplified circuit expressions that may include replacement of active circuit elements with ideal controlled voltage and current sources. As such, simulation with macromodels should be treated as 'typical' performance and not relied upon as final proof-of-design. Use of macromodel descriptions is not a substitute for worst-case design analysis, nor for testing real circuits over temperature, supply, and other operating limits.

The output format is provided as ASCII text netlists suitable for generic SPICE. This format is compatible with most versions of SPICE such as PSPICE and HSPICE. Additional information is found in HFAN 6.1 *Input/Output Models for Maxim Fiber Components*.

To extract the circuit netlists using the Adobe Acrobat Reader follow these instructions. Select the "Text Select Tool" by clicking the left mouse button on this icon of the menu bar (a capital T with a small dashed box to the lower right). Highlight the desired netlist text with the cursor. Use the copy command from the edit menu to capture the selected lines. Then paste the selected lines into a text file editor and save the file with an extension compatible with the simulator.

Revision A0, July 30, 2004

# I/O Models for the MAX3640

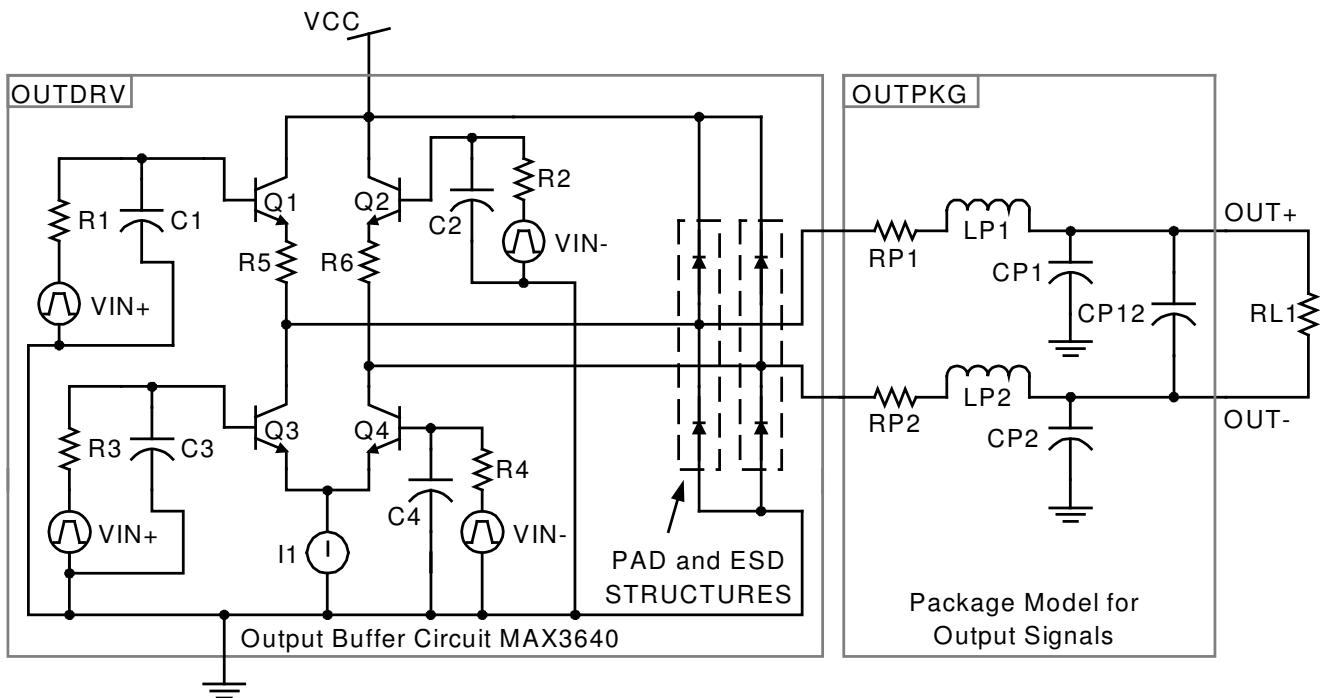


Figure 1. Output model for signals DOA1 to DOA4 and DOB1 to DOB4 for the MAX3640.

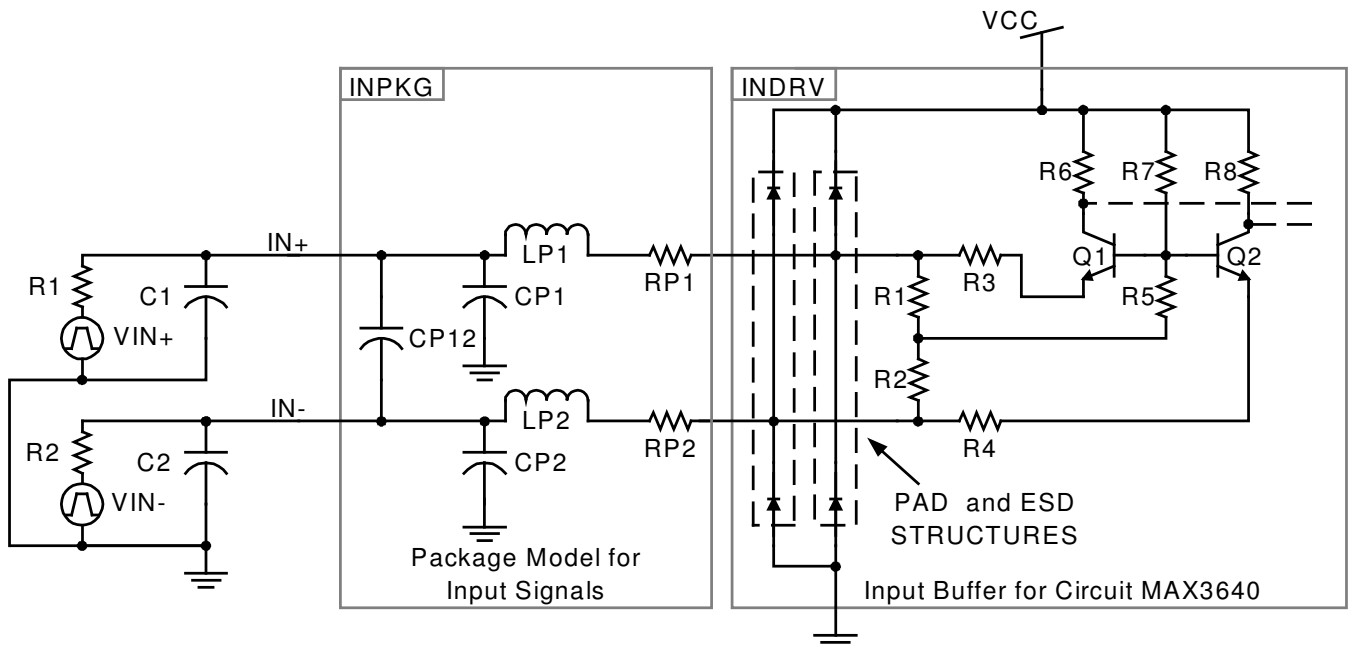


Figure 2. Input model for signals DIA1 to DIA4 and DIB1 to DIB4 for the MAX3640.

## Notes:

The schematics on the previous page represent the output and input stage of the Maxim MAX3640 622 Mbps Crosspoint Switch. The output circuit shown is for the signal outputs (DOA1+ to DOA4+, DOB1+ to DOB4+, DOA1- to DOA4-, DOB1- DOB4-) and the input circuit is shown with the signal inputs (DIA1+ to DIA4+, DOB1+ to DIB4+, DIA1- to DIA4-, DIB1- DIB4-). However the models are given in generic SPICE, which only accepts node names as numbers. As discussed in the application note the output signals are described as (2001, 2002) and the input signals are described as (2101, 2102). These models are only valid at 25°C. The bias currents for the input and output circuitry are modeled by ideal current sources. This model is not compensated for variations in VCC, so VCC equal to 3.3V should be used.

**The Output Stage:** The output stage of the MAX3640 is shown as the sub-circuits “OUTDRV” and “OUTPKG”.

**The OUTDRV Sub-circuit:** The driver sub-circuit is a simplified version of the output stage used by the MAX3640 Limiting Amplifier. The output load is configured with a 100Ω differential load. The common mode output voltage is set to 1.2V. The differential peak to peak output voltage is approximately 650mV. The waveform is a pulse whose period is 3.238ns with rise and fall times approximately 250ps. The netlist is given in SPICE 2G6 format in Appendix A.

**The Input Stage:** The input structure of the MAX3640 connects to a common emitter configuration. The input stage has sub-circuits “INDRV” and “INPKG”.

**The INDRV Sub-circuit:** The input structure of the MAX3640 is connected to an equivalent resistive, capacitive and inductive network of the input package. The driving voltage source should be set to 0V differential at t=0. This ensures that the two AC coupling capacitors are not charged to different voltages initially (this is the way the circuit operates in steady-state operation). This was achieved by using a piecewise linear source as the driver. See Appendix B for the input netlist.

**Text File Format:** This model is shipped in “pdf” format. Models and netlists can be copied to text format in the Acrobat Reader by holding the left mouse button on the “Text Select Tool.” Then the user can “select” what netlist and/or subcircuit with the mouse. Then use the copy command from the “edit” menu to capture the selected lines. These lines can then be “pasted” into the user’s text file.

# Appendix A: Output Netlist

\* 3640 Output Model

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.OPT ACCT NOMOD LIMPTS=10000

.TEMP 25

.OP

.TRAN 2P 10n

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\* Voltage Source

VCC 101 0 3.3

\* Load Resistance

\*RL1 101 2001 50

\*RL2 101 2002 50

RL1 2001 2002 100

\*\*\*\*\*

XOUTPKG 2001 2002 50 51 OUTPKG

XOUTDRV 50 51 101 OUTDRV

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.SUBCKT OUTDRV 50 51 101

VIN1 1 0 PULSE (2.42 2.62 0n .3n .3n 1.3n 3.238n)

R1 2 1 50

C1 2 0 .1p

VIN2 3 0 PULSE (2.62 2.42 0n .3n .3n 1.3n 3.238n)

R2 4 3 50

C2 4 0 .1p

VIN3 5 0 PULSE (.9 1 .2n .3n .3n 1.3n 3.238n)

R3 6 5 50

C3 6 0 .1p

VIN4 7 0 PULSE (1 .9 .2n .3n .3n 1.3n 3.238n)

R4 8 7 50

C4 8 0 .1p

R5 9 50 45

R6 10 51 45

XQ1 101 2 9 0 H12A04\_4

XQ2 101 4 10 0 H12A04\_4

XQ3 50 8 11 0 H12A04

XQ4 51 6 11 0 H12A04

I1 11 0 20mA

\* Pad and ESD Structures  
XD1 50 101 0 HDE113032  
XD2 0 50 0 HDE113032  
XD3 51 101 0 HDE113032  
XD4 0 51 0 HDE113032  
XP1 50 0 HPAD3  
XP2 51 0 HPAD3

.ENDS OUTDRV

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.SUBCKT OUTPKG 2001 2002 50 51

RP1 50 500 340M  
RP2 51 501 340M  
LP1 500 2001 .83N  
LP2 501 2002 .83N  
CP1 2001 0 178F  
CP2 2002 0 178F  
CP12 2001 2002 1F

.ENDS OUTPKG

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\* Transistor Model

.SUBCKT H12A04\_4 1 2 3 21

CP1EPI 1 2 23.208F

CP1P2 12 3 39.329F

CTRENCH 1 20 38.268F

RBX 2 12 10.277 TC=2.663M

RCX 1 10 11.754 TC=2.354M,979.573N

RCI 10 11 618.653M TC=2.354M,979.573N

REX 13 3 1.397 TC=123.150U

RSUB 20 21 2.607K

QP 20 10 12 20 TXP 4 OFF

QN 11 12 13 11 TX 4

.MODEL TX NPN( IS=1.663E-017 XTI=3 EG=1.140 BF=232.533 BR=20 XTB=450M

+ VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=63.273M

+ IKR=1.159M ISE=7.865E-021 ISC=1.011E-029 RB=41.109 RBM=30.832

+ IRB=10.112M CJE=53.836F MJE=490M VJE=940M FC=990M CJC=10.965F

+ MJC=470M VJC=850M TF=3.778P TR=19N XTF=1 VTF=1K ITF=29.811M PTF=5

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+ KF=1.500F AF=1 )
.MODEL TXP PNP( IS=9.840E-019 CJE=10.965F MJE=470M VJE=850M
CJC=11.603F
+ MJC=400M VJC=650M BF=10K BR=832.864U TF=1N FC=900M )
.ENDS H12A04_4
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* Transistor Model
.SUBCKT H12A04 1 2 3 21
CP1EPI 1 2 5.802F
CP1P2 12 3 9.832F
CTRENCH 1 20 9.567F
RBX 2 12 41.109 TC=2.663M
RCX 1 10 47.018 TC=2.354M,979.573N
RCI 10 11 2.475 TC=2.354M,979.573N
REX 13 3 5.590 TC=123.150U
RSUB 20 21 10.427K
QP 20 10 12 20 TXP OFF
QN 11 12 13 11 TX
.MODEL TX NPN( IS=1.663E-017 XTI=3 EG=1.140 BF=232.533 BR=20 XTB=450M
+ VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=63.273M
+ IKR=1.159M ISE=7.865E-021 ISC=1.011E-029 RB=41.109 RBM=30.832
+ IRB=10.112M CJE=53.836F MJE=490M VJE=940M FC=990M CJC=10.965F
+ MJC=470M VJC=850M TF=3.778P TR=19N XTF=1 VTF=1K ITF=29.811M PTF=5
+ KF=1.500F AF=1 )
.MODEL TXP PNP( IS=9.840E-019 CJE=10.965F MJE=470M VJE=850M
CJC=11.603F
+ MJC=400M VJC=650M BF=10K BR=832.864U TF=1N FC=900M )
.ENDS H12A04
*****

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* ESD Diode Model
.SUBCKT HDE113032 1 2 21
CP1EPI 1 4 88.881F
QD 5 4 1 5 QESD
RS 4 2 2.531 TC=2.729M,1.896U
RSUB 5 21 2.936K
CTRENCH 2 5 22.961F
.MODEL QESD PNP( IS=1.181E-017 NF=1.050 BF=800M BR=600U CJE=155.018F
+ VJE=600M MJE=400M CJC=53.258F VJC=650M MJC=400M )
.ENDS HDE113032
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* Pad Model
.SUBCKT HPAD3 1 3
CPAD 1 10 86.407F
REPI 10 20 149.204M TC=4.800M,5U
CTRENCH 21 20 79.795F
DS 21 20 DSUB
RS 3 21 369.115
.MODEL DSUB D( IS=98.719F CJO=555.750F M=400M VJ=650M )
.ENDS HPAD3
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.PROBE
.END
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# Appendix B: Input Netlist

\* 3640 Input Model

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.OPT ACCT NOMOD LIMPTS=10000

.TEMP 25

.OP

.TRAN 2P 5n

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\* Voltage Source

VCC 101 0 3.3

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\* Add input source here.

\* The source should connect to node 2101 (VINP)

\* and 2102 (VINN).

\* Example:

VINP 50 0 PULSE (1.3 1.1 .2n .4n .4n 1.2n 3.21548n)

VINN 60 0 PULSE (1.1 1.3 .2n .4n .4n 1.2n 3.21548n)

RL1 2101 50 50

RL2 2102 60 50

CL1 2101 0 1p

CL2 2102 0 1p

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XINPKG 2101 2102 1001 1002 INPKG

XINDRV 1001 1002 101 INDRV

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.SUBCKT INDRV 1001 1002 101

R1 1001 1 50

R2 1002 1 50

R3 3 1001 1.5k

R4 4 1002 1.5k

R5 2 1 5k

R6 101 5 1125

R7 101 2 5k

R8 101 6 1125

XQ1 5 2 3 0 H11M02

XQ2 6 2 4 0 H11M02

\* Pad and ESD Structures  
XD1 1001 101 0 HDE113032  
XD2 0 1001 0 HDE113032  
XD3 1002 101 0 HDE113032  
XD4 0 1002 0 HDE113032  
XP1 1001 0 HPAD3  
XP2 1002 0 HPAD3

.ENDS INDRV

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.SUBCKT INPKG 2101 2102 1001 1002

RP1 1001 2002 340M  
RP2 1002 2003 340M  
LP1 2002 2101 .83N  
LP2 2003 2102 .83N  
CP1 2101 0 178F  
CP2 2102 0 178F  
CP12 2101 2102 1F

.ENDS INPKG

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\* Transistor Model

.SUBCKT H11M02 1 2 3 21

CP1EPI 1 2 9.985E-016

CP1P2 12 3 1.848F

CTRENCH 1 20 4.783F

RBX 2 12 271.456 TC=2.588M

RCX 1 10 186.577 TC=3.250M,2.039U

RCI 10 11 9.820 TC=3.250M,2.039U

REX 13 3 39.087 TC=44.406U

RSUB 20 21 26.178K

QP 20 10 12 20 TXP OFF

QN 11 12 13 11 TX

.MODEL TX NPN( IS=1.920E-018 XTI=3 EG=1.140 BF=265 BR=20 XTB=450M  
VAF=29

+ VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=6.878M IKR=126U

+ ISE=9.083E-022 ISC=1.168E-030 RB=271.456 RBM=203.592 IRB=1.168M

+ CJE=6.452F MJE=490M VJE=940M FC=990M CJC=1.729F MJC=470M

VJC=850M

+ TF=3.651P TR=19N XTF=1 VTF=1K ITF=3.568M PTF=5 KF=1.500F AF=1 )

.MODEL TXP PNP( IS=1.680E-019 CJE=1.729F MJE=470M VJE=850M CJC=3.870F

+ MJC=400M VJC=650M BF=10K BR=664.767U TF=1N FC=900M )  
.ENDS H11M02

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\* ESD Diode Model

.SUBCKT HDE113032 1 2 21

CP1EPI 1 4 88.881F

QD 5 4 1 5 QESD

RS 4 2 2.531 TC=2.729M,1.896U

RSUB 5 21 2.936K

CTRENCH 2 5 22.961F

.MODEL QESD PNP( IS=1.181E-017 NF=1.050 BF=800M BR=600U CJE=155.018F

+ VJE=600M MJE=400M CJC=53.258F VJC=650M MJC=400M )

.ENDS HDE113032

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\* Pad Model

.SUBCKT HPAD3 1 3

CPAD 1 10 86.407F

REPI 10 20 149.204M TC=4.800M,5U

CTRENCH 21 20 79.795F

DS 21 20 DSUB

RS 3 21 369.115

.MODEL DSUB D( IS=98.719F CJO=555.750F M=400M VJ=650M )

.ENDS HPAD3

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.PROBE

.END