

## MAX3268 I/O Model

SPICE I/O Macromodels aid in understanding signal integrity issues in electronic systems. Most of Maxim's High Frequency/Fiber Communication ICs utilize input and output (I/O) circuits with Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) formats to transfer data into and out of an IC. These models are based on simplified circuit expressions that may include replacement of active circuit elements with ideal controlled voltage and current sources. As such, simulation with macromodels should be treated as 'typical' performance and not relied upon as final proof-of-design. Use of macromodel descriptions is not a substitute for worst-case design analysis, nor for testing real circuits over temperature, supply, and other operating limits.

The output format is provided as ASCII text netlists suitable for generic SPICE. This format is compatible with most versions of SPICE such as PSPICE and HSPICE. Additional information is found in HFAN 6.1 *Input/Output Models for Maxim Fiber Components*.

To extract the circuit netlists using the Adobe Acrobat Reader follow these instructions. Select the "Text Select Tool" by clicking the left mouse button on this icon of the menu bar (a capital T with a small dashed box to the lower right). Highlight the desired netlist text with the cursor. Use the copy command from the edit menu to capture the selected lines. Then paste the selected lines into a text file editor and save the file with an extension compatible with the simulator.

Version A, Jan 21, 2003

Version A1, May25, 2003

## I/O Models for the MAX3268 Limiting Amplifier

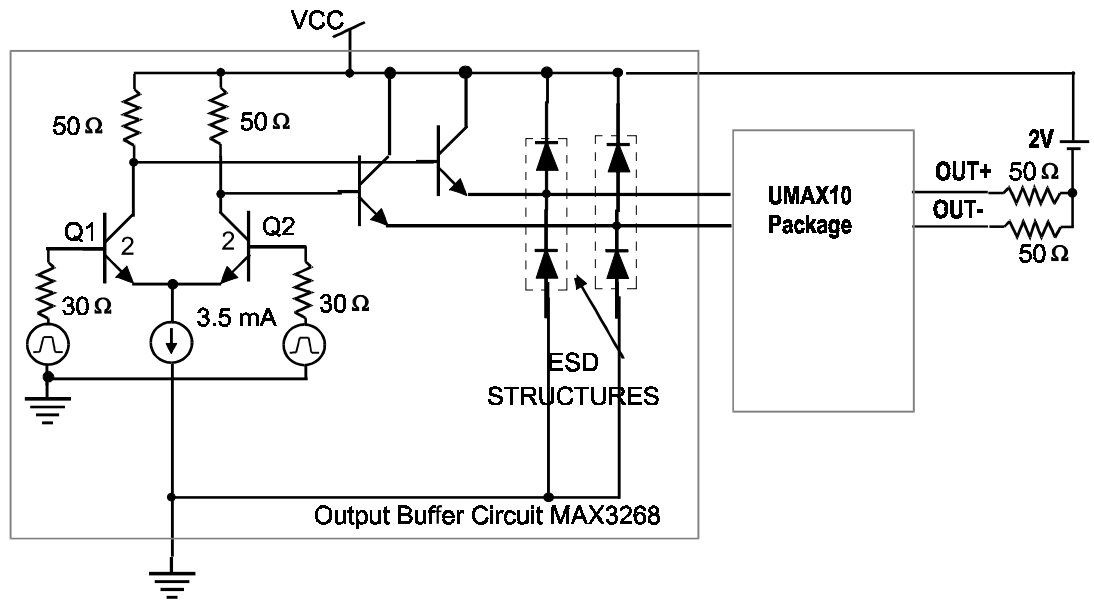


Figure 1. Output stage for the MAX3268 including a simplified package model.

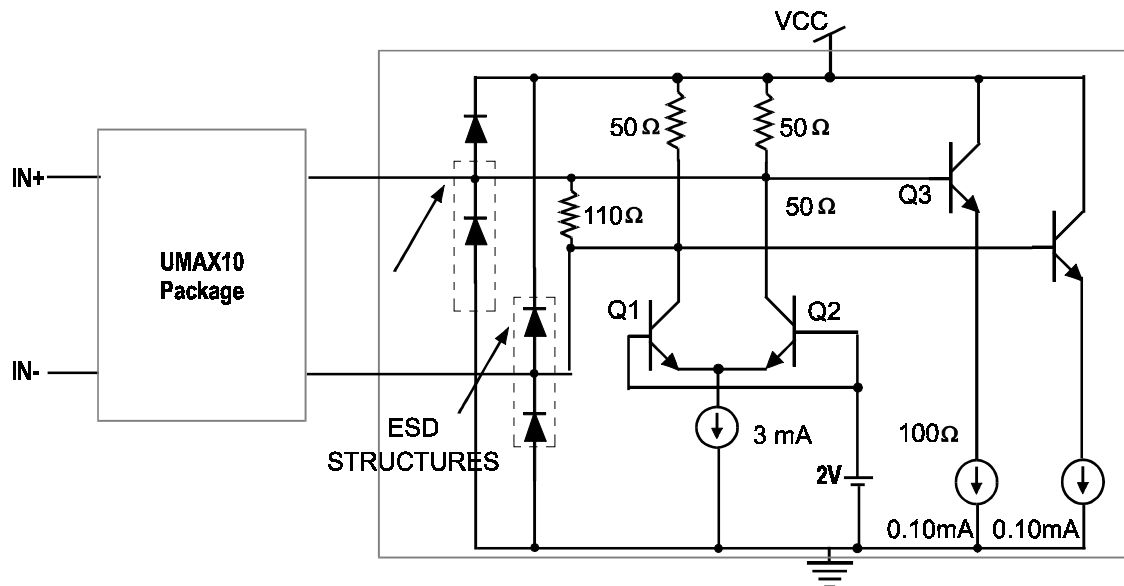


Figure 2. Simplified input package model and input circuitry for the MAX3268.

## Notes:

### MAX3268 Input Model

The input structure of the MAX3268 is connected to a differential common-emitter amplifier that is designed to compensate for internal device mismatches. In the actual circuit there is a feedback path that controls the differential amplifier to adjust the input biasing points and compensate for any device mismatch. This model does not attempt to model the offset correction functionality, but the amplifier is included to account for any parasitic impedance that it presents to the input pins.

The input pins are nodes 101 (IN+) and 102 (IN-). These are connected to a model pattern generator that includes  $50\Omega$  output impedance and AC coupling. The pattern generator has two  $1M\Omega$  resistors connected to ground to provide a DC path to ground at these nodes, which is a requirement of the Spice simulator.

The driving voltage source (VIN) should be set to 0V differential at  $t=0$ . This ensures that the two AC coupling capacitors are not charged to different voltages initially. (This is the way the circuit operates in steady-state operation.) I achieved this condition by using a piecewise linear source as my driver, with a voltage of 0V at  $t=0$ . The swing applied to the input can be varied across the acceptable range of input for the MAX3268, which is  $10mV_{P-P}$  to  $1200mV_{P-P}$ . Remember that there is a 50% drop across the  $50\Omega$  output impedance of the generator, so to get a  $10mV_{P-P}$  swing at the input the MAX3269 the source should swing between  $+10mV$  and  $-10mV$  (a  $20mV_{P-P}$  swing).

### MAX3268 PECL Output Model

The PECL output model is a simplified version of the output stage used by the MAX3268 limiting amplifier. The package model is quite accurate, and the output impedance presented by the output emitter-followers should also be fairly accurate. Simplifications have been made regarding performance over temperature, so the model is only accurate at a temperature of  $35^{\circ}C$ . Operation at other temperatures will give very different results than the actual MAX3268 output. The model was not compensated for variation in VCC, so  $VCC=3.3V$  should be used.

The output pins are nodes 2001 (OUT-) and 2002 (OUT+). In order to see the signal at the output a PECL load of  $50\Omega$  to  $(VCC - 2V)$  has been included. This is the external termination and not included on the MAX3268. Replace this load with the interconnect model for signal integrity simulations.

The signal source for the PECL output is VSOURCE1 and VSOURCE2. It is important that there is no differential voltage between the inputs at  $t=0$ , so PWL source was used that starts

both sources a 0V. This is very important to get the correctly initialize the operating conditions of the circuit. Signal swing should be from  $-100\text{mV}$  to  $+100\text{mV}$  for each VSOURCE1 and VSOURCE2, and these sources need to be complementary.

**Text File Format:** This model is shipped in “pdf” format. Models and netlists can be copied to text format in the Acrobat Reader by holding the left mouse button on the “Text Select Tool.” Then the user can “select” what netlist and/or subcircuit with the mouse. Then use the copy command from the “edit” menu to capture the selected lines. These lines can then be “pasted” into the user’s text file. Make sure to save the text tile as plain text without any formatting.

## Circuit Netlist – Input circuit

INPUT - MAX3268 INPUT CIRCUIT

\*  
\* THIS IS THE TYPICAL INPUT OF THE MAX3268  
\* IN+ IS NODE 101 AND IN- IS NODE 102  
\*

.OPTIONS ACCT NOMOD NOPAGE LIMPTS=1000000 RELTOL=.001

.WIDTH OUT=80

.TEMP 35

.OP

.TRAN 2P 1.7N

\* DRIVER \*\*\*\*\*  
VIN 81 82 PWL(0 0 50P 600M 350P 600M 500P -600M 750P -600M 900P 600M)  
R6 81 91 50  
R5 82 92 50  
C1 91 101 0.1U  
C2 92 102 0.1U  
R21 81 0 1MEG  
R22 82 0 1MEG  
\*\*\*\*\*

VCC 1 0 DC 3.3

XESD1P 1001 1 0 HDE113032  
XESD1M 0 1001 0 HDE113032  
XESD2P 1002 1 0 HDE113032  
XESD2M 0 1002 0 HDE113032

XR1 1001 1 0 HRND520  
XR2 1002 1 0 HRND520  
XR3 1001 1002 0 HRND110

XPK1 0 101 102 0 0 0 0 0 0 0 1001 1002 0 0 0 0 0 0 0 0 0 0 UMAX10

XQ1a 1001 3 4 0 H11M05  
XQ1b 1001 3 4 0 H11M05  
XQ1c 1001 3 4 0 H11M05

XQ2a 1002 3 4 0 H11M05  
XQ2b 1002 3 4 0 H11M05  
XQ2c 1002 3 4 0 H11M05

XQ3a 1 1001 2001 0 H12A05  
XQ3b 1 1001 2001 0 H12A05

XQ4a 1 1002 2002 0 H12A05  
XQ4b 1 1002 2002 0 H12A05

I1 4 0 3M  
I2 2002 0 1M  
I3 2001 0 1M  
VOFFSET 3 0 2

\*\*\*\*\*

.SUBCKT H12A05 1 2 3 21  
CP1EPI 1 2 7.147F  
CP1P2 12 3 12.915F  
CTRENCH 1 20 10.524F  
RBX 2 12 30.538 TC=2.649M  
RCX 1 10 35.869 TC=2.315M,931.161N  
RCI 10 11 1.888 TC=2.315M,931.161N  
REX 13 3 4.328 TC=182.441U  
RSUB 20 21 9.008K  
QP 20 10 12 20 TXP OFF  
QN 11 12 13 11 TX  
.MODEL TX NPN( IS=2.302E-017 XTI=3 EG=1.140 BF=223.719 BR=20 XTB=450M  
+ VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=88.032M  
+ IKR=1.613M ISE=1.089E-020 ISC=1.400E-029 RB=30.538 RBM=22.904  
+ IRB=14M CJE=74.302F MJE=490M VJE=940M FC=990M CJC=14.718F MJC=470M  
+ VJC=850M TF=3.814P TR=19N XTF=1 VTF=1K ITF=40.860M PTF=5 KF=1.500F  
+ AF=1 )  
.MODEL TXP PNP( IS=1.308E-018 CJE=14.718F MJE=470M VJE=850M CJC=13.849F  
+ MJC=400M VJC=650M BF=10K BR=869.864U TF=1N FC=900M )  
.ENDS H12A05

\*\*\*\*\*

\*\*\*\*\*

.SUBCKT H11M05 1 2 3 21  
CP1EPI 1 2 2.192F  
CP1P2 12 3 6.473F  
CTRENCH 1 20 7.654F  
RBX 2 12 164.841 TC=1.611M  
RCX 1 10 40.687 TC=2.961M,1.642U  
RCI 10 11 2.141 TC=2.961M,1.642U  
REX 13 3 7.711 TC=57.819U  
RSUB 20 21 14.233K  
QP 20 10 12 20 TXP OFF  
QN 11 12 13 11 TX  
.MODEL TX NPN( IS=1.151E-017 XTI=3 EG=1.140 BF=223.719 BR=20 XTB=450M  
+ VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=44.016M  
+ IKR=806.400U ISE=5.444E-021 ISC=7.000E-030 RB=164.841 RBM=123.631  
+ IRB=7M CJE=37.151F MJE=490M VJE=940M FC=990M CJC=7.359F MJC=470M  
+ VJC=850M TF=3.814P TR=19N XTF=1 VTF=1K ITF=20.430M PTF=5 KF=1.500F  
+ AF=1 )  
.MODEL TXP PNP( IS=6.540E-019 CJE=7.359F MJE=470M VJE=850M CJC=7.985F  
+ MJC=400M VJC=650M BF=10K BR=924.230U TF=1N FC=900M )  
.ENDS H11M05

\*\*\*\*\*

\*\*\*\*\*

\* TSPICE CONVERSION TO SPICE2G.6  
\*created Fri May 10 14:56:27 2002

```

*
*
.SUBCKT HDE113032 1 2 21
CP1EPI 1 4 88.881F
QD 5 4 1 5 QESD
RS 4 2 2.531 TC=2.729M,1.896U
RSUB 5 21 2.936K
CTRENCH 2 5 22.961F
.MODEL QESD PNP( IS=1.181E-017 NF=1.050 BF=800M BR=600U CJE=155.018F
+ VJE=600M MJE=400M CJC=53.258F VJC=650M MJC=400M )
.ENDS HDE113032
*****
*****
* TSPICE CONVERSION TO SPICE2G.6
*created Tue Jul 02 11:07:54 2002
*
*
.SUBCKT HRND520 1 2 3
R1 1 4 260 TC=150U
R2 4 2 260 TC=150U
C1 1 3 82.558F
C2 4 3 165.116F
C3 2 3 82.558F
.ENDS HRND520
*****
*****
* TSPICE CONVERSION TO SPICE2G.6
*created Tue Jul 02 09:55:20 2002
*
*
.SUBCKT HRND110 1 2 3
R1 1 4 55 TC=150U
R2 4 2 55 TC=150U
C1 1 3 52.896F
C2 4 3 105.793F
C3 2 3 52.896F
.ENDS HRND110
*****
*****
.SUBCKT UMAX10 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
* Pad->Lead Frame side 2 Lead Pin 1 Chip side 12
* Pad->Lead Frame side 3 Lead Pin 2 Chip side 13
* Pad->Lead Frame side 4 Lead Pin 3 Chip side 14
* Pad->Lead Frame side 5 Lead Pin 4 Chip side 15
* Pad->Lead Frame side 6 Lead Pin 5 Chip side 16
* Pad->Lead Frame side 7 Lead Pin 6 Chip side 17
* Pad->Lead Frame side 8 Lead Pin 7 Chip side 18
* Pad->Lead Frame side 9 Lead Pin 8 Chip side 19
* Pad->Lead Frame side 10 Lead Pin 9 Chip side 20
* Pad->Lead Frame side 11 Lead Pin 10 Chip side 21
* Padtop -> 22
* Padbot -> 23

```

\* GND -> 24

\*

\* resistors

\*

RB01 12 25 47M  
RB02 13 26 41M  
\*RB02 13 26 200M  
RB03 14 27 38M  
\*RB03 14 27 200M  
RB04 15 28 38M  
RB05 16 29 46M  
RB06 17 30 44M  
RB07 18 31 38M  
RB08 19 32 37M  
RB09 20 33 40M  
RB10 21 34 47M

\*

\* inductors

\*

LLAP\_1\_11 2 25 1.54e-009  
LLAP\_2\_12 3 26 1.35e-009  
LLAP\_3\_13 4 27 1.25e-009  
LLAP\_4\_14 5 28 1.27e-009  
LLAP\_5\_15 6 29 1.49e-009  
LLAP\_6\_16 7 30 1.49e-009  
LLAP\_7\_17 8 31 1.26e-009  
LLAP\_8\_18 9 32 1.23e-009  
LLAP\_9\_19 10 33 1.35e-009  
LLAP\_10\_20 11 34 1.54e-009  
KLAP\_1\_2 LLAP\_1\_11 LLAP\_2\_12 0.34261  
KLAP\_1\_3 LLAP\_1\_11 LLAP\_3\_13 0.176584  
KLAP\_1\_4 LLAP\_1\_11 LLAP\_4\_14 0.0915267  
KLAP\_1\_5 LLAP\_1\_11 LLAP\_5\_15 0.0564433  
KLAP\_2\_3 LLAP\_2\_12 LLAP\_3\_13 0.335633  
KLAP\_2\_4 LLAP\_2\_12 LLAP\_4\_14 0.162671  
KLAP\_2\_5 LLAP\_2\_12 LLAP\_5\_15 0.0958912  
KLAP\_3\_4 LLAP\_3\_13 LLAP\_4\_14 0.329375  
KLAP\_3\_5 LLAP\_3\_13 LLAP\_5\_15 0.168531  
KLAP\_4\_5 LLAP\_4\_14 LLAP\_5\_15 0.306046  
KLAP\_6\_7 LLAP\_6\_16 LLAP\_7\_17 0.314557  
KLAP\_6\_8 LLAP\_6\_16 LLAP\_8\_18 0.170634  
KLAP\_6\_9 LLAP\_6\_16 LLAP\_9\_19 0.0958912  
KLAP\_6\_10 LLAP\_6\_16 LLAP\_10\_20 0.054925  
KLAP\_7\_8 LLAP\_7\_17 LLAP\_8\_18 0.329341  
KLAP\_7\_9 LLAP\_7\_17 LLAP\_9\_19 0.161015  
KLAP\_7\_10 LLAP\_7\_17 LLAP\_10\_20 0.0890176  
KLAP\_8\_9 LLAP\_8\_18 LLAP\_9\_19 0.343007  
KLAP\_8\_10 LLAP\_8\_18 LLAP\_10\_20 0.17874  
KLAP\_9\_10 LLAP\_9\_19 LLAP\_10\_20 0.347465

\* LB11 22 23 11P

\*

\* capacitors

\*

C01 2 24 193F

```

C02 3 24 164F
C03 4 24 163F
C04 5 24 164F
C05 6 24 193F
C06 7 24 193F
C07 8 24 165F
C08 9 24 163F
C09 10 24 164F
C10 11 24 193F
*
* mutual capacitors
*
C01_02 2 3 60.300F
C02_03 3 4 58.700F
C03_04 4 5 58.700F
C04_05 5 6 60.300F
C06_07 7 8 60.300F
C07_08 8 9 58.800F
C08_09 9 10 58.700F
C09_10 10 11 60.300F
.ENDS UMAX10
*****

.PRINT TRAN V(101) V(102)

.END

```

## Circuit Netlist – Output circuit

```

INPUT - MAX3268 PECL OUTPUT CIRCUIT
*
* THIS IS THE TYPICAL PECL OUTPUT OF THE MAX3268
* OUT+ IS NODE 2002 AND OUT- IS NODE 2001
*
* This an adaptation of the MAX3269 PCEL output. The rise and fall
* time of the MAX3268 is slower than the MAX3269.
* The source has been changed to reflect this. Bob Sparkes (20/01/03)
.OPTIONS LIMPTS=1000000
.WIDTH OUT=80
.TEMP 35
.OP
.TRAN 2P 1.4N
* DRIVER *****
VOFFSET 66 0 2
VSOURCE1 11 66 PWL(0 0 50P 100M 350P 100M 500P -100M 750P -100M 900P 100M)
VSOURCE2 22 66 PWL(0 0 50P -100M 350P -100M 500P 100M 750P 100M 800P -100M)
R4 22 2 30
R5 11 1 30
*****
VCC 101 0 DC 3.3
XESD1P 1001 1 0 HDE113032
XESD1M 0 1001 0 HDE113032
XESD2P 1002 1 0 HDE113032
XESD2M 0 1002 0 HDE113032
R1 101 100 4
XR2 100 3 0 HRND120

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XR3 100 4 0 HRND120
XQ1A 3 1 111 0 H12A04
XQ1B 3 1 111 0 H12A04
XQ2A 4 2 111 0 H12A04
XQ2B 4 2 111 0 H12A04
XQ3A 101 3 1001 0 H14E04
XQ3B 101 3 1001 0 H14E04
XQ4A 101 4 1002 0 H14E04
XQ4B 101 4 1002 0 H14E04
*I1 111 0 7M
I1 111 0 3.5M
C1 3 0 70F
C2 4 0 70F
XPAK 0 0 0 0 0 0 0 0 2001 2002 0 0 0 0 0 0 0 0 1001 1002 0 0 0 0 UMAX10
***** PECL LOAD*****
R7 2001 999 50
R8 2002 999 50
V2 101 999 2
*****
*****
* TSPICE CONVERSION TO SPICE2G.6
*created Tue Jul 02 16:15:07 2002
*
.SUBCKT UMAX10 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
*
* Pad->Lead Frame side 2 Lead Pin 1 Chip side 12
* Pad->Lead Frame side 3 Lead Pin 2 Chip side 13
* Pad->Lead Frame side 4 Lead Pin 3 Chip side 14
* Pad->Lead Frame side 5 Lead Pin 4 Chip side 15
* Pad->Lead Frame side 6 Lead Pin 5 Chip side 16
* Pad->Lead Frame side 7 Lead Pin 6 Chip side 17
* Pad->Lead Frame side 8 Lead Pin 7 Chip side 18
* Pad->Lead Frame side 9 Lead Pin 8 Chip side 19
* Pad->Lead Frame side 10 Lead Pin 9 Chip side 20
* Pad->Lead Frame side 11 Lead Pin 10 Chip side 21
* Padtop -> 22
* Padbot -> 23
* GND -> 24
*
* resistors
*
RB01 12 25 47M
RB02 13 26 41M
RB03 14 27 38M
RB04 15 28 38M
RB05 16 29 46M
RB06 17 30 44M
RB07 18 31 38M
RB08 19 32 37M
RB09 20 33 40M
RB10 21 34 47M
*
* inductors
*
LLAP_1_11 2 25 1.54e-009
LLAP_2_12 3 26 1.35e-009
LLAP_3_13 4 27 1.25e-009
LLAP_4_14 5 28 1.27e-009
LLAP_5_15 6 29 1.49e-009
LLAP_6_16 7 30 1.49e-009
LLAP_7_17 8 31 1.26e-009

```

```

LLAP_8_18 9 32 1.23e-009
LLAP_9_19 10 33 1.35e-009
LLAP_10_20 11 34 1.54e-009
KLAP_1_2 LLAP_1_11 LLAP_2_12 0.34261
KLAP_1_3 LLAP_1_11 LLAP_3_13 0.176584
KLAP_1_4 LLAP_1_11 LLAP_4_14 0.0915267
KLAP_1_5 LLAP_1_11 LLAP_5_15 0.0564433
KLAP_2_3 LLAP_2_12 LLAP_3_13 0.335633
KLAP_2_4 LLAP_2_12 LLAP_4_14 0.162671
KLAP_2_5 LLAP_2_12 LLAP_5_15 0.0958912
KLAP_3_4 LLAP_3_13 LLAP_4_14 0.329375
KLAP_3_5 LLAP_3_13 LLAP_5_15 0.168531
KLAP_4_5 LLAP_4_14 LLAP_5_15 0.306046
KLAP_6_7 LLAP_6_16 LLAP_7_17 0.314557
KLAP_6_8 LLAP_6_16 LLAP_8_18 0.170634
KLAP_6_9 LLAP_6_16 LLAP_9_19 0.0958912
KLAP_6_10 LLAP_6_16 LLAP_10_20 0.054925
KLAP_7_8 LLAP_7_17 LLAP_8_18 0.329341
KLAP_7_9 LLAP_7_17 LLAP_9_19 0.161015
KLAP_7_10 LLAP_7_17 LLAP_10_20 0.0890176
KLAP_8_9 LLAP_8_18 LLAP_9_19 0.343007
KLAP_8_10 LLAP_8_18 LLAP_10_20 0.17874
KLAP_9_10 LLAP_9_19 LLAP_10_20 0.347465
* LB11 22 23 11P
*
* capacitors
*
C01 2 24 193F
C02 3 24 164F
C03 4 24 163F
C04 5 24 164F
C05 6 24 193F
C06 7 24 193F
C07 8 24 165F
C08 9 24 163F
C09 10 24 164F
C10 11 24 193F
*
* mutual capacitors
*
C01_02 2 3 60.300F
C02_03 3 4 58.700F
C03_04 4 5 58.700F
C04_05 5 6 60.300F
C06_07 7 8 60.300F
C07_08 8 9 58.800F
C08_09 9 10 58.700F
C09_10 10 11 60.300F
.ENDS UMAX10
*****
*****
* TSPICE CONVERSION TO SPICE2G.6
*created Thu Jul 04 10:48:33 2002
*
*
.SUBCKT HRND120 1 2 3
R1 1 4 59.938 TC=150U
R2 4 2 59.938 TC=150U
C1 1 3 8.400F
C2 4 3 16.800F
C3 2 3 8.400F

```

```
.ENDS HRND120
*****
*****
* TSPICE CONVERSION TO SPICE2G.6
*created Fri May 10 14:56:27 2002
*
*
.SUBCKT HDE113032 1 2 21
CP1EPI 1 4 88.881F
QD 5 4 1 5 QESD
RS 4 2 2.531 TC=2.729M,1.896U
RSUB 5 21 2.936K
CTRENCH 2 5 22.961F
.MODEL QESD PNP( IS=1.181E-017 NF=1.050 BF=800M BR=600U CJE=155.018F
+ VJE=600M MJE=400M CJC=53.258F VJC=650M MJC=400M )
.ENDS HDE113032
*****
*****
.SUBCKT H12A04 1 2 3 21
CP1EPI 1 2 5.802F
CP1P2 12 3 9.832F
CTRENCH 1 20 9.567F
RBX 2 12 41.109 TC=2.663M
RCX 1 10 47.018 TC=2.354M,979.573N
RCI 10 11 2.475 TC=2.354M,979.573N
REX 13 3 5.590 TC=123.150U
RSUB 20 21 10.427K
QP 20 10 12 20 TXP OFF
QN 11 12 13 11 TX
.MODEL TX NPN( IS=1.663E-017 XTI=3 EG=1.140 BF=232.533 BR=20 XTB=450M
+ VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=63.273M
+ IKR=1.159M ISE=7.865E-021 ISC=1.011E-029 RB=41.109 RBM=30.832
+ IRB=10.112M CJE=53.836F MJE=490M VJE=940M FC=990M CJC=10.965F
+ MJC=470M VJC=850M TF=3.778P TR=19N XTF=1 VTF=1K ITF=29.811M PTF=5
+ KF=1.500F AF=1 )
.MODEL TXP PNP( IS=9.840E-019 CJE=10.965F MJE=470M VJE=850M CJC=11.603F
+ MJC=400M VJC=650M BF=10K BR=832.864U TF=1N FC=900M )
.ENDS H12A04
*****
*****
.SUBCKT H14E04 1 2 3 21
CP1EPI 1 2 12.185F
CP1P2 12 3 19.634F
CTRENCH 1 20 15.307F
RBX 2 12 20.554 TC=2.663M
RCX 1 10 23.509 TC=2.354M,979.573N
RCI 10 11 1.237 TC=2.354M,979.573N
REX 13 3 2.795 TC=123.150U
RSUB 20 21 6.195K
QP 20 10 12 20 TXP OFF
QN 11 12 13 11 TX
.MODEL TX NPN( IS=3.326E-017 XTI=3 EG=1.140 BF=232.533 BR=20 XTB=450M
+ VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=126.546M
+ IKR=2.318M ISE=1.573E-020 ISC=2.022E-029 RB=20.554 RBM=15.416
+ IRB=20.223M CJE=107.672F MJE=490M VJE=940M FC=990M CJC=21.929F
+ MJC=470M VJC=850M TF=3.778P TR=19N XTF=1 VTF=1K ITF=59.621M PTF=5
+ KF=1.500F AF=1 )
.MODEL TXP PNP( IS=1.968E-018 CJE=21.929F MJE=470M VJE=850M CJC=21.582F
+ MJC=400M VJC=650M BF=10K BR=809.067U TF=1N FC=900M )
.ENDS H14E04
*****
*****
```

```
.PRINT TRAN V(2001) V(2002)  
.END
```