



RELIABILITY REPORT
FOR
MAX9451EHJ+
PLASTIC ENCAPSULATED DEVICES

October 23, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Approved by
Ken Wendel
Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX9451EHJ+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description	V.Quality Assurance Information
II.Manufacturing Information	VI.Reliability Evaluation
III.Packaging Information	IV.Die Information
.....Attachments	

I. Device Description

A. General

The MAX9450/MAX9451/MAX9452 clock generators provide high-precision clocks for timing in SONET/SDH systems or Gigabit Ethernet systems. The MAX9450/MAX9451/MAX9452 can also provide clocks for the high-speed and high-resolution ADCs and DACs in 3G base stations. Additionally, the devices can also be used as a jitter attenuator for generating high-precision CLK signals. The MAX9450/MAX9451/MAX9452 feature an integrated VCXO. This configuration eliminates the use of an external VCXO and provides a cost-effective solution for generating high-precision clocks. The MAX9450/MAX9451/MAX9452 feature two differential inputs and clock outputs. The inputs accept LVPECL, LVDS, differential signals, and LVCMOS. The input reference clocks range from 8kHz to 500MHz. The MAX9450/MAX9451/MAX9452 offer LVPECL, HSTL, and LVDS outputs, respectively. The output range is up to 160MHz, depending on the selection of crystal. The input and output frequency selection is implemented through the I²C or SPI(tm) interface. The MAX9450/MAX9451/MAX9452 feature clock output jitter less than 0.8ps RMS (in a 12kHz to 20MHz band) and phase-noise attenuation greater than -130dBc/Hz at 100kHz. The phase-locked loop (PLL) filter can be set externally, and the filter bandwidth can vary from 1Hz to 20kHz. The MAX9450/MAX9451/MAX9452 feature an input clock monitor with a hitless switch. When a failure is detected at the selected reference clock, the device can switch to the other reference clock. The reaction to the recovery of the failed reference clock can be revertive or nonrevertive. If both reference clocks fail, the PLL retains its nominal frequency within a range of ± 20 ppm at +25°C. The MAX9450/MAX9451/MAX9452 operate from 2.4V to 3.6V supply and are available in 32-pin TQFP packages with exposed pads.

II. Manufacturing Information

A. Description/Function:	High-Precision Clock Generators with Integrated VCXO
B. Process:	TS35
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Philippines
F. Date of Initial Production:	July 22, 2006

III. Packaging Information

A. Package Type:	32-pin TQFP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2120
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Multi Layer Theta Ja:	36°C/W
K. Multi Layer Theta Jc:	4°C/W

IV. Die Information

A. Dimensions:	87 X 88 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35μm
F. Minimum Metal Spacing:	0.35μm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- | | |
|-----------------------------------|---|
| A. Quality Assurance Contacts: | Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 46 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 23.4 \times 10^{-9}$$
$$\lambda = 23.4 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the TS35 Process results in a FIT Rate of 0.11 @ 25C and 1.93 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The EC39-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX9451EHJ+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	46	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data