

RELIABILITY REPORT
FOR
MAX8842ELT+
PLASTIC ENCAPSULATED DEVICES

January 28, 2010

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX8842ELT+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX8840/MAX8841/MAX8842 ultra-low-noise, low-dropout (LDO) linear regulators are designed to deliver up to 150mA continuous output current. These regulators achieve a low 120mV dropout for 120mA load current. The MAX8840 uses an advanced architecture to achieve ultra-low output voltage noise of 11 μ V_{RMS} and PSRR of 54dB at 100kHz. The MAX8841 does not require a bypass capacitor, hence achieving the smallest PC board area. The MAX8842 output voltage can be adjusted with an external divider. The MAX8840/MAX8841 are preset to a variety of voltages in the 1.5V to 4.5V range. Designed with a p-channel MOSFET series pass transistor, the MAX8840/MAX8841/MAX8842 maintain very low ground current (40 μ A). The regulators are designed and optimized to work with low-value, low-cost ceramic capacitors. The MAX8840 requires only 1 μ F (typ) of output capacitance for stability with any load. When disabled, current consumption drops to below 1 μ A. The MAX8840/MAX8841/MAX8842 are available in a tiny 1mm x 1.5mm x 0.8mm μ DFN.

II. Manufacturing Information

A. Description/Function:	Ultra-Low-Noise, High PSRR, Low-Dropout, 150mA Linear Regulators in μ DFN
B. Process:	B8
C. Number of Device Transistors:	
D. Fabrication Location:	California or Texas
E. Assembly Location:	Thailand
F. Date of Initial Production:	January 20, 2007

III. Packaging Information

A. Package Type:	6-pin uDFN
B. Lead Frame:	Substrate
C. Lead Finish:	Gold
D. Die Attach:	Non-conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2565
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Multi Layer Theta Ja:	477°C/W

IV. Die Information

A. Dimensions:	31 X 30 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 47 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.8 \times 10^{-9}$$
$$\lambda = 22.8 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the B8 Process results in a FIT Rate of 0.06 @ 25C and 0.99 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The PM21-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX8842ELT+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	47	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-55°C/125°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data