

RELIABILITY REPORT  
FOR  
MAX8660ETL+T  
PLASTIC ENCAPSULATED DEVICES

August 26, 2011

**MAXIM INTEGRATED PRODUCTS**

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## Conclusion

The MAX8660ETL+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX8660/MAX8661 power management ICs (PMICs) power applications processors (APs) in smart cellular phones, PDAs, Internet appliances, and other portable devices. Four step-down DC-DC outputs, three linear regulators, and an 8th always-on LDO are integrated with power-management functions. Two dynamically controlled DC-DC outputs power the processor core and internal memory. Two other DC-DC converters power I/O, memory, and other peripherals. Additional functions include on/off control for outputs, low-battery detection, reset output, and a 2-wire I<sup>2</sup>C serial interface. The MAX8661 functions the same as the MAX8660, except it lacks the REG1 step-down regulator and the REG7 linear regulator. All step-down DC-to-DC outputs use fast 2MHz PWM switching and tiny external components. They automatically switch from PWM to high-efficiency, light-load operation to reduce operating current and extend battery life. In addition, a forced-PWM option allows low-noise operation at all loads. Overvoltage lockout protects the device against inputs up to 7.5V.

## II. Manufacturing Information

A. Description/Function:	High-Efficiency, Low- $I_{sub}Q$ , PMICs with Dynamic Voltage Management for Mobile Applications
B. Process:	S45
C. Number of Device Transistors:	36000
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	China, Taiwan and Thailand
F. Date of Initial Production:	July 22, 2006

## III. Packaging Information

A. Package Type:	40-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2068
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	45°C/W
K. Single Layer Theta Jc:	2°C/W
L. Multi Layer Theta Ja:	28°C/W
M. Multi Layer Theta Jc:	2°C/W

## IV. Die Information

A. Dimensions:	132 X 127 mils
B. Passivation:	$Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	$SiO_2$
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)  
Don Lipps (Manager, Reliability Engineering)  
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 0 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$

$$\lambda = 22.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing (lot TN10G3080B, D/C 0932)

The PP41 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2000V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78.

**Table 1**  
Reliability Evaluation Test Results

**MAX8660ETL+T**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	SN10DQ002A, D/C 0622

Note 1: Life Test Data may represent plastic DIP qualification lots.