

RELIABILITY REPORT
FOR
MAX8550ETI+
PLASTIC ENCAPSULATED DEVICES

May 19, 2009

MAXIM INTEGRATED PRODUCTS

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Approved by
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Conclusion

The MAX8550ETI+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX8550/MAX8551 integrate a synchronous-buck PWM controller to generate VDDQ, a sourcing and sinking LDO linear regulator to generate VTT, and a 10mA reference output buffer to generate VTTR. The buck controller drives two external N-channel MOSFETs to generate output voltages down to 0.7V from a 2V to 28V input with output currents up to 15A. The LDO can sink or source up to 1.5A continuous and 3A peak current. Both the LDO output and the 10mA reference buffer output can be made to track the REFIN voltage. These features make the MAX8550/MAX8551 ideally suited for DDR memory applications in desktops, notebooks, and graphic cards. The PWM controller in the MAX8550/MAX8551 utilizes Maxim's proprietary Quick-PWM(tm) architecture with programmable switching frequencies of up to 600kHz. This control scheme handles wide input/output voltage ratios with ease and provides 100ns response to load transients while maintaining high efficiency and a relatively constant switching frequency. The MAX8550 offers fully programmable UVP/OVP and skip-mode options ideal in portable applications. Skip mode allows for improved efficiency at lighter loads. The MAX8551, which is targeted towards desktop and graphic-card applications, does not offer the pulse-skip feature. The VTT and VTTR outputs track to within 1% of VREFIN / 2. The high bandwidth of this LDO regulator allows excellent transient response without the need for bulk capacitors, thus reducing cost and size. The buck controller and LDO regulators are provided with independent current limits. Adjustable lossless foldback current limit for the buck regulator is achieved by monitoring the drain-to-source voltage drop of the low-side MOSFET. Additionally, overvoltage and undervoltage protection mechanisms are built in. Once the overcurrent condition is removed, the regulator is allowed to enter soft-start again. This helps minimize power dissipation during a short-circuit condition. The MAX8550/MAX8551 allow flexible sequencing and standby power management using the SHDNA-bar, SHDNB-bar, and STBY inputs. Both the MAX8550 and MAX8551 are available in a small 5mm x 5mm, 28-pin thin QFN package.

II. Manufacturing Information

A. Description/Function:	Integrated DDR Power-Supply Solutions for Desktops, Notebooks, and Graphic Cards
B. Process:	B8
C. Number of Device Transistors:	
D. Fabrication Location:	Texas
E. Assembly Location:	ASAT China, UTL Thailand, Unisem Malaysia
F. Date of Initial Production:	January 24, 2004

III. Packaging Information

A. Package Type:	28-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0706
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	47°C/W
K. Single Layer Theta Jc:	2.1°C/W
L. Multi Layer Theta Ja:	29°C/W
M. Multi Layer Theta Jc:	2.1°C/W

IV. Die Information

A. Dimensions:	98 X 125 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/0.5% Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 383 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 2.80 \times 10^{-9}$$

$$\lambda = 2.80 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at <http://www.maxim-ic.com/>. Current monitor data for the B8 Process results in a FIT Rate of 1.86 @ 25C and 22.5 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The PN27 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX8550ETI+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	383	0
Moisture Testing (Note 2) 85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2) Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data