MAX821TUS
Rev. A

RELIABILITY REPORT

FOR

MAX821TUS

PLASTIC ENCAPSULATED DEVICES

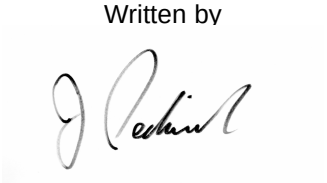
August 24, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

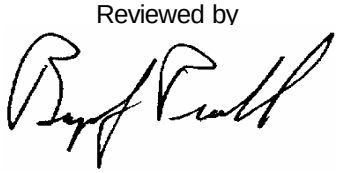
SUNNYVALE, CA 94086

Written by



Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl
Quality Assurance
Managing Executive Director

Conclusion

The MAX821T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX821T microprocessor (µP) supervisory circuit monitors power supplies in µP and digital systems. It provides excellent circuit reliability and low cost by eliminating external components and adjustments when used with 5V-powered or 3V-powered circuits. The MAX821 also provides a power-on reset timeout delay that is pin selectable to 1ms (max), 20ms (min), or 100ms (min).

This device performs a single function: it asserts a reset signal whenever the V_{CC} supply voltage falls below a preset threshold, and it keeps reset asserted for the pin-selected reset timeout delay after V_{CC} has risen above the reset threshold. The MAX 821T has an active-low /RESET output (which is guaranteed to be in the correct state for V_{CC} down to 1V). The reset comparator is designed to ignore fast transients on V_{CC}. Reset thresholds suitable for operation with a variety of supply voltages are available.

Low supply current make the MAX821T ideal for use in portable equipment.

B. Absolute Maximum Ratings

Item	Rating
Terminal Voltage (with respect to GND)	
V_{CC}	-0.3V to 6.0V
All Other Inputs	-0.3V to (V_{CC} + 0.3V)
Input Current, V_{CC}, SRT	20mA
Output Current, RESET or /RESET	20mA
Storage Temp.	-65°C to +160°C
Operating Temperature Range	-40°C to +85°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
4-Pin SOT143	320mW
Derates above +70°C	
4-Pin SOT143	4.0mW/°C

II. Manufacturing Information

A. Description/Function:	4-Pin µP Voltage Monitor with Pin-Selectable Power-On Reset Timeout Delay
B. Process:	B12/S12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	492
D. Fabrication Location:	Oregon or California, USA
E. Assembly Location:	Malaysia or Thailand
F. Date of Initial Production:	January, 1997

III. Packaging Information

A. Package Type:	4 Lead SOT-143
B. Lead Frame:	Alloy 42
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1601-0007
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	44 x 31 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 240 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 4.58 \times 10^{-9}$

$\lambda = 4.58$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-4556) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B12/S12 process results in a FIT rate of 0.10 @ 25°C and 1.78 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The MS04 die type has been found to have all pins able to withstand a transient pulse of ±2000V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX821TUS

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		240	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT143	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

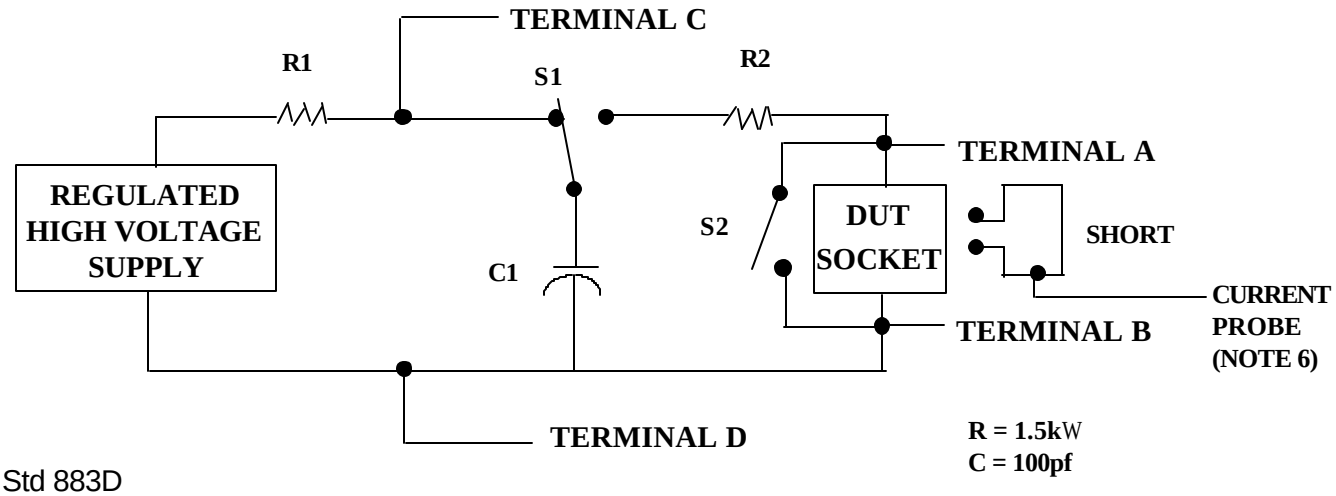
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

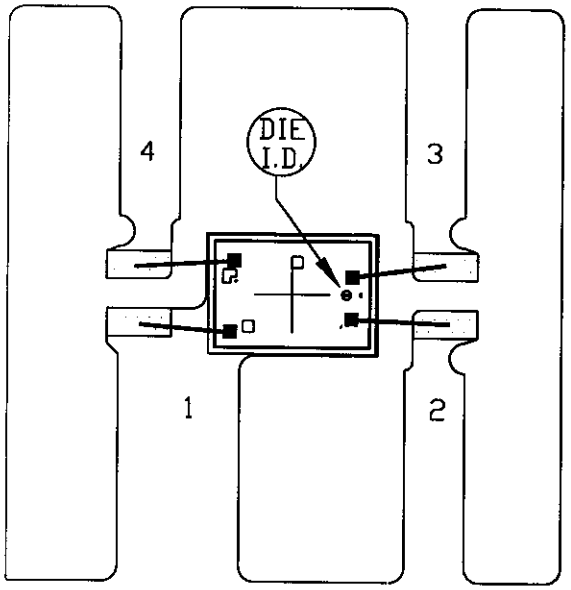
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



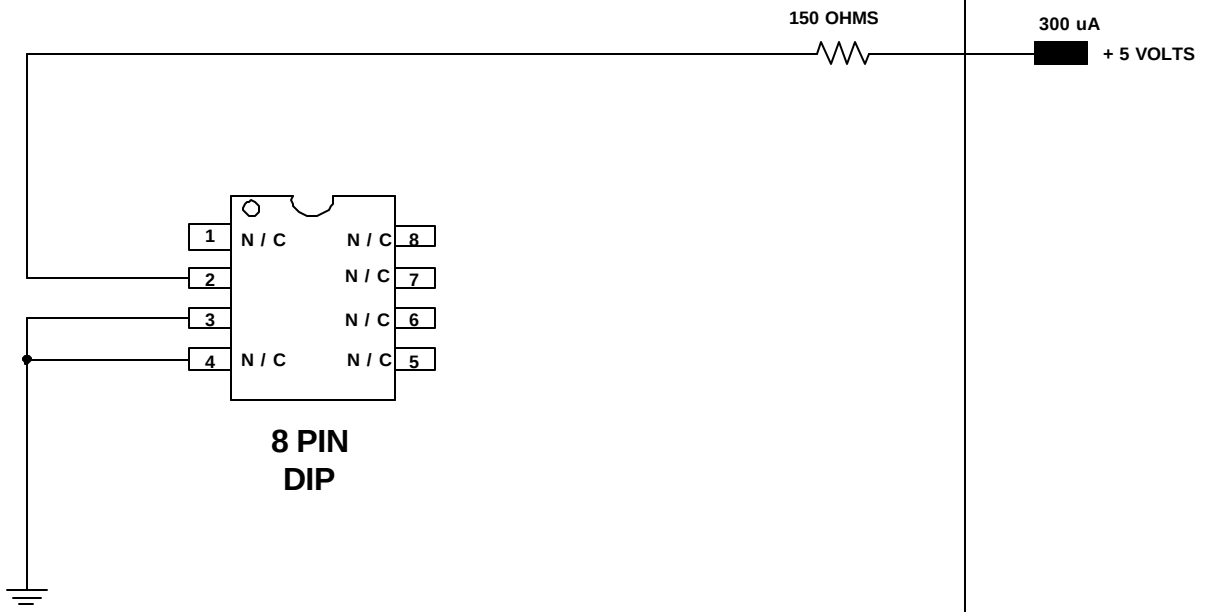
Mil Std 883D
Method 3015.7
Notice 8



PKG.CODE: U4-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 45X32	PKG. DESIGN			BUILDSHEET NUMBER: 05-1601-0007 / REV.: B

ONCE PER SOCKET

ONCE PER BOARD



8 PIN DIP

DEVICES: MAX 705/706/707/708/709/809/811/812/813/821/822/6314/6315/6326/6327/6328
MAX. EXPECTED CURRENT = 300 uA

NOTES: MS17 only for MAX 6326-28