

RELIABILITY REPORT
FOR
MAX703xxA
PLASTIC ENCAPSULATED DEVICES

October 21, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX703 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX703 microprocessor (μ P) supervisory circuit reduces the complexity and number of components required to monitor power-supply and battery functions in μ P systems. This device significantly improves system reliability and accuracy compared to separate ICs or discrete components.

The MAX703 provides multiple functions, including an active-low reset, a manual reset input, a power-fail comparator, and battery-backup switching. The MAX703 generates a reset when the supply drops below 4.65V

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Terminal Voltage (with respect to GND)	
V_{CC}	-0.3V to 6.0V
VBATT	-0.3V to 6.0V
All Other Inputs (Note 1)	-0.3V to (VCB+0.3V)
Continuous Input Current	
V_{CC}	200mA
VBATT	50mA
GND	20mA
Output Current	
/RESET, /PFO	18mA
V_{OUT}	100mA
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
8-Pin NSO	471mW
8-Pin DIP	727mw
Derates above +70°C	
8-Pin NSO	5.88mW/°C
8-Pin DIP	9.09mW/°C

II. Manufacturing Information

A. Description/Function:	3.0V/3.3V μ P Supervisory Circuit
B. Process:	S3 (SG3) - Standard 3 micron silicon gate CMOS
C. Number of Device Transistors:	802
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Philippines, Malaysia, Thailand or Korea
F. Date of Initial Production:	March, 1994

III. Packaging Information

A. Package Type:	8 Lead NSO	8-Lead PDIP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mi dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1701-0141	#05-1701-0142
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	

IV. Die Information

A. Dimensions:	80 x110 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 1190 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 0.91 \times 10^{-9} \quad \lambda = 0.91 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-0526) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PY07-2 die type has been found to have all pins able to withstand a transient pulse of $\pm 1500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$ and/or $\pm 20\text{V}$.

Table 1
Reliability Evaluation Test Results

MAX703xxA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		1190	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality (generic test vehicle)	PDIP NSO	600 2239	0 18
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality (generic test vehicle)		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Small Outline package.

Note 2: Generic Process/Package data

Attachment #3

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

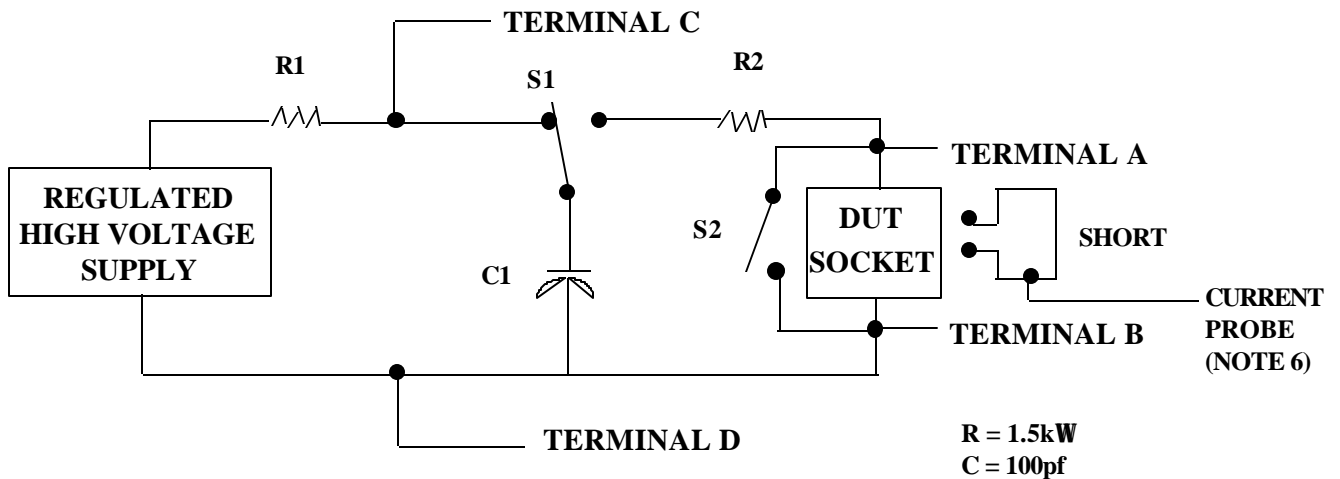
2/ No connects are not to be tested.

3/ Repeat pin combination 1 for each named Power supply and for ground

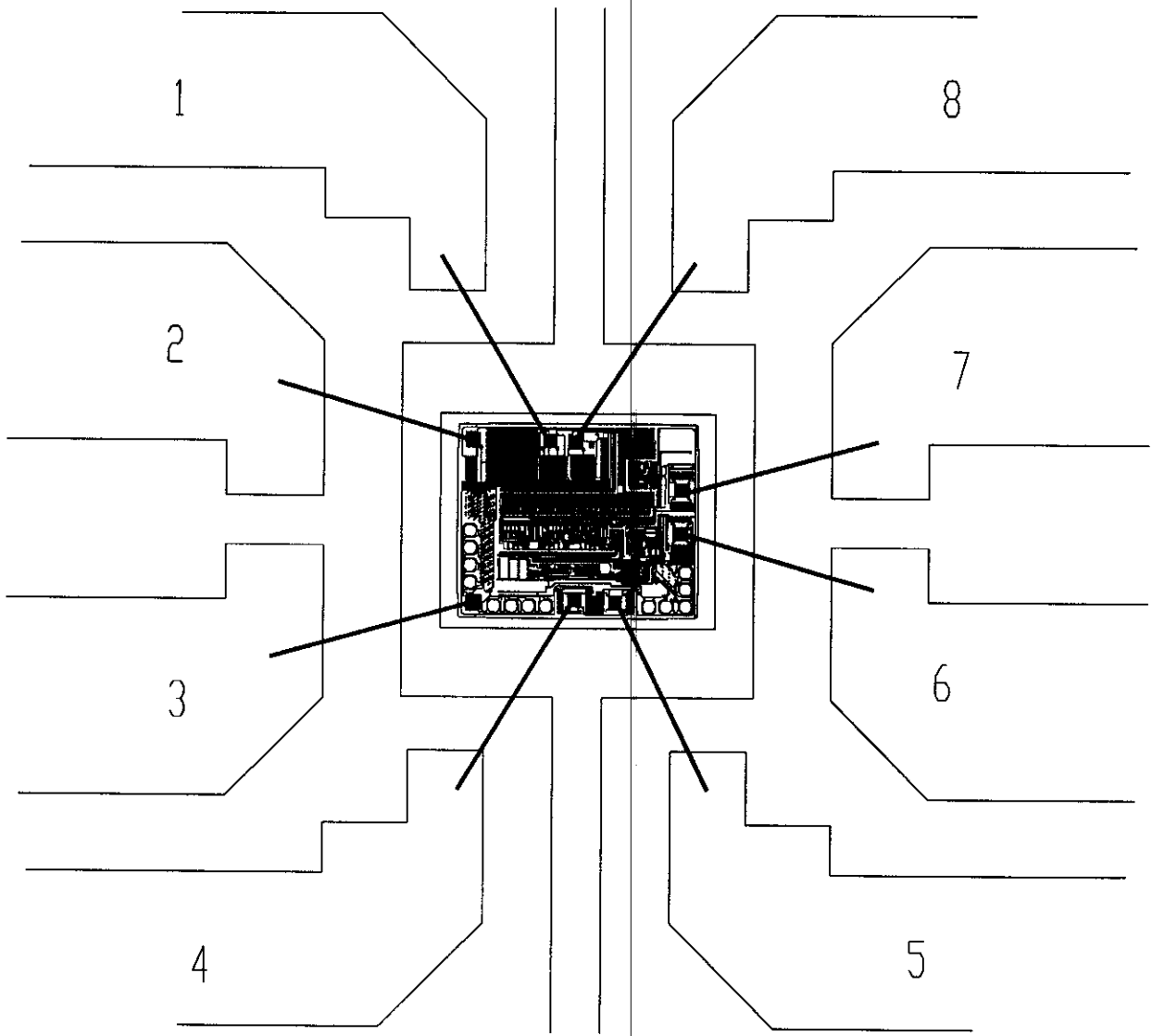
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

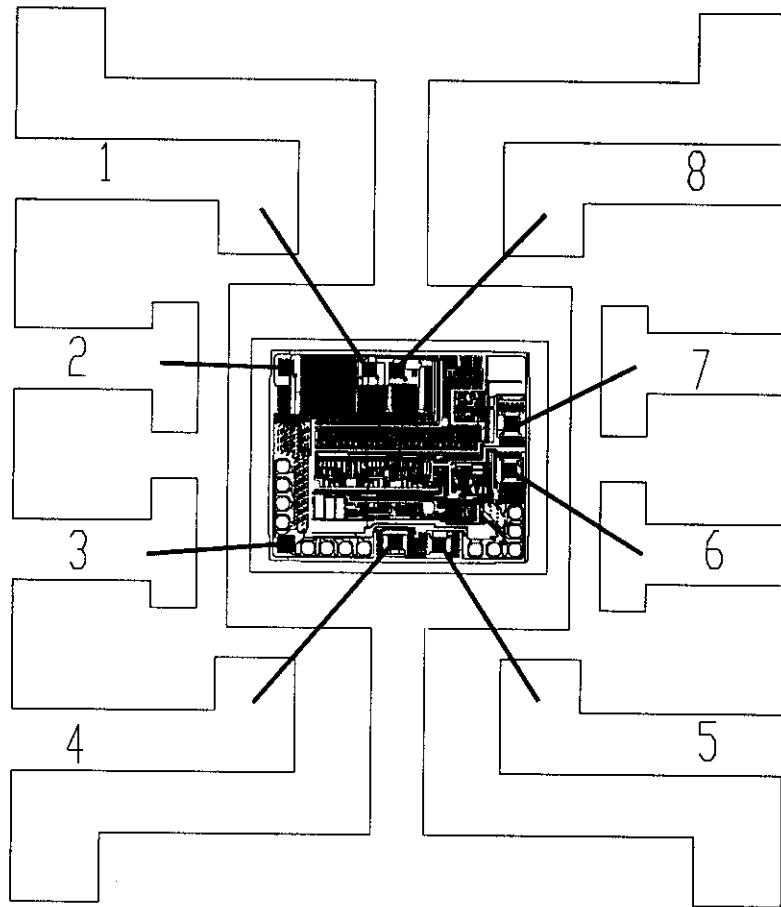
- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of



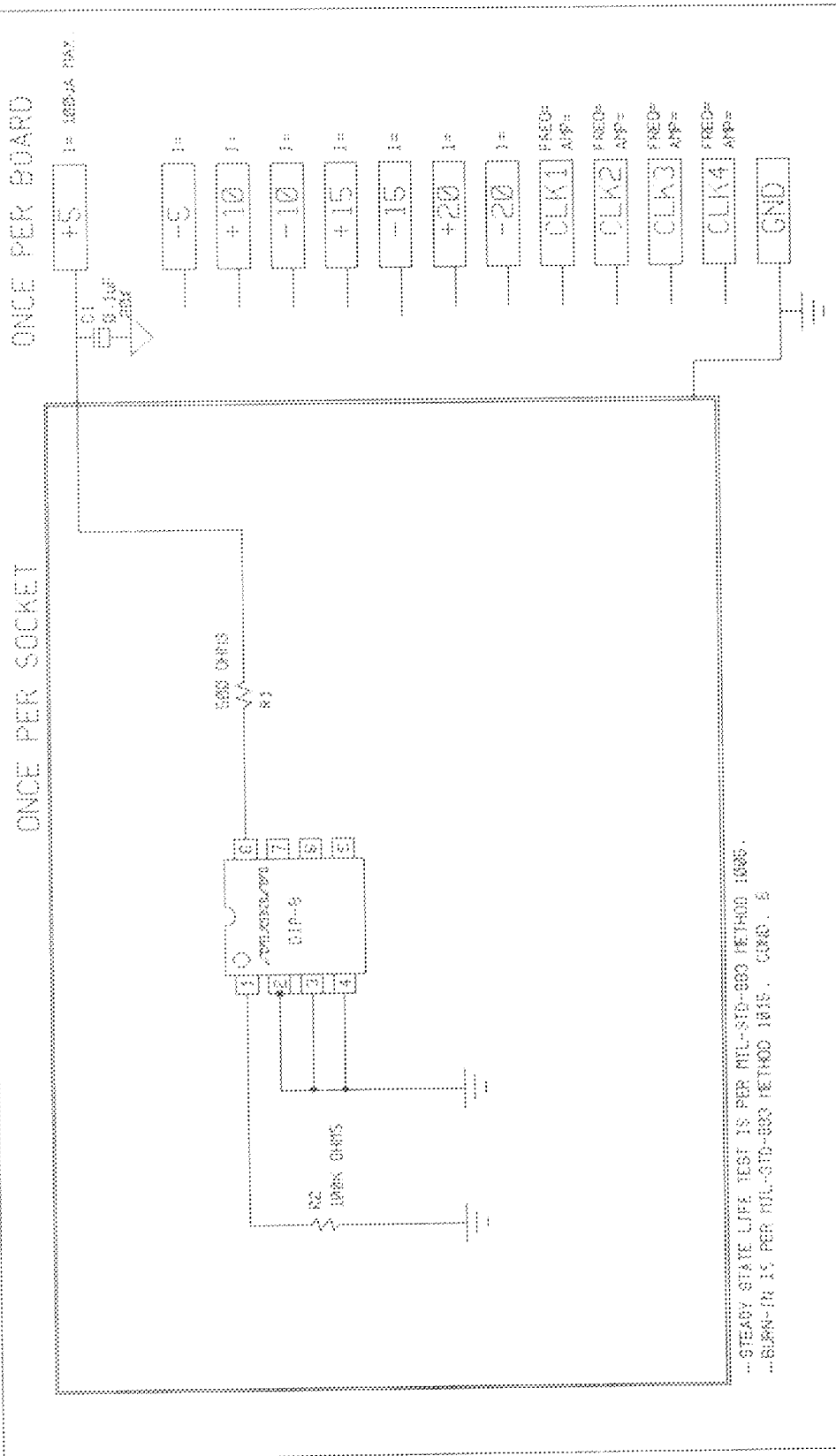
all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



PKG.CODE: P8-1		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 100 X 100	PKG. DESIGN		3/10/93	BUILDSHEET NUMBER:	REV.:
			4/1/93	05-1701-0141	A



PKG.CODE: S8-2		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 90 X 90	PKG.	[REDACTED]	3/10/93	BUILDSHEET NUMBER:	REV.:
	DESIGN		4/1/93	05-1701-0142	A



-- STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1008.
 -- BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. B

NOTES:	SPEC. NO. 06-526 REV. E	MAXIM BURN-IN SCHEMATIC
1. TEMPERATURE: 125C OR EQUIVALENT 2. TIME: 168 HOURS MIN. OR EQUIVALENT 3. ALL COMPONENTS AND MATERIAL MUST STAND 155C ENVIRONMENT	DATE: 11/24/95	DEVICE TYPE: MAX980/698A/692/693A/694 MAX200/781/783/784/790 MAX984/885/895 MAX 917/818/819
4. APPROVED FOR EXH COMMERCIAL EX 1 HR/883	DRAWN BY: C. JONES	