

RELIABILITY REPORT
FOR
MAX4925ELT+
PLASTIC ENCAPSULATED DEVICES

July 10, 2008

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
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Approved by
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Quality Assurance
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Conclusion

The MAX4925ELT+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4923-MAX4926 overvoltage protection (OVP) controllers protect low-voltage systems against high-voltage faults of up to +28V with an appropriate external pFET. When the input voltage exceeds the overvoltage lockout (OVLO) threshold, or falls below the undervoltage lockout (UVLO) threshold, these devices turn off the pFET to prevent damage to protected components and issue a flag to notify the processor of a fault condition. The typical overvoltage trip level is set to 7.18V (MAX4923), 6.16V (MAX4924), 5.65V (MAX4925), and 4.46V (MAX4926). The undervoltage trip level is set to 2.44V (typ) for all devices. The input (IN) is ESD protected to $\pm 15\text{kV}$ HBM when bypassed to ground with a 1 μF ceramic capacitor. All devices are offered in a small, 6-pin (1.5mm x 1.0mm) μDFN package and are specified over the extended -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	Overvoltage Protectors with External pFET
B. Process:	B8
C. Number of Device Transistors:	
D. Fabrication Location:	California or Texas
E. Assembly Location:	Thailand
F. Date of Initial Production:	April 20, 2007

III. Packaging Information

A. Package Type:	6-pin uDFN
B. Lead Frame:	Substrate
C. Lead Finish:	Gold
D. Die Attach:	Non-conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2204
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	°C/W
K. Single Layer Theta Jc:	°C/W
L. Multi Layer Theta Ja:	477°C/W
M. Multi Layer Theta Jc:	°C/W

IV. Die Information

A. Dimensions:	31 X 30 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 24.43 \times 10^{-9}$$

$$\lambda = 24.43 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6633) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1N). Current monitor data for the S4 Process results in a FIT Rate of 0.09 @ 25C and 1.61 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The AS76-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/-500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX4925ELT+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
Moisture Testing (Note 2) 85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2) Temperature Cycle	-55°C/125°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data