

RELIABILITY REPORT
FOR
MAX490ExxA
PLASTIC ENCAPSULATED DEVICES

July 8, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX490E successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX490E is a low-power transceivers for RS-485 and RS-422 communications in harsh environments. Each driver output and receiver input is protected against $\pm 15\text{kV}$ electrostatic discharge (ESD) shocks, without latchup. This parts contains one driver and one receiver. The driver slew rate of the MAX490E is not limited, allowing it to transmit up to 2.5Mbps.

This transceivers draw as little as $120\mu\text{A}$ supply current when unloaded or when fully loaded with disabled drivers (see Selection Table)..

Drivers are short-circuit current limited, and are protected against excessive power dissipation by thermal shutdown circuitry that places their outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The MAX490E is designed for full-duplex communications.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Supply Voltage (VCC)	12V
Control Input Voltage (RE, DE)	-0.5V to (VCC + 0.5V)
Driver Input Voltage (DI)	-0.5V to (VCC + 0.5V)
Driver Output Voltage (Y, Z; A, B)	-8V to +12.5V
Receiver Input Voltage (A, B)	-8V to +12.5V
Receiver Output Voltage (RO)	-0.5V to (VCC + 0.5V)
Operating Temperature Ranges	
MAX490EC__	0°C to +70°C
MAX480EE__	-40°C to +85°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°
Continuous Power Dissipation (TA = +70°C)	
8-Pin Plastic DIP	727mW
8-Pin NSO	471mW
Derate above +70°C	
8-Pin Plastic DIP	9.09mW/°C
8-Pin NSO	5.88mW/°C

II. Manufacturing Information

- A. Description/Function: $\pm 15\text{kV}$ ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceiver
- B. Process: S3 (Standard 3 micron silicon gate CMOS)
- C. Number of Device Transistors: 295
- D. Fabrication Location: Oregon or California, USA
- E. Assembly Location: Philippines, Malaysia or Thailand
- F. Date of Initial Production: January, 1994

III. Packaging Information

- | A. Package Type: | 8-Lead PDIP | 8-Lead NSO |
|---|--------------------------|--------------------------|
| B. Lead Frame: | Copper | Copper |
| C. Lead Finish: | Solder Plate | Solder Plate |
| D. Die Attach: | Silver-filled Epoxy | Silver-filled Epoxy |
| E. Bondwire: | Gold (1.3 mil dia.) | Gold (1.3 mil dia.) |
| F. Mold Material: | Epoxy with silica filler | Epoxy with silica filler |
| G. Assembly Diagram: | # 05-1901-0138 | # 05-1901-0139 |
| H. Flammability Rating: | Class UL94-V0 | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: | Level 1 | Level 1 |

IV. Die Information

- A. Dimensions: 85 x 128 mils
- B. Passivation: $\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 3 microns (as drawn)
- F. Minimum Metal Spacing: 3 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric: SiO_2
- I. Die Separation Method: Wafer Saw

V. Quality Assurance Information


- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 160 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

 Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 6.79 \times 10^{-9}$$

$$\lambda = 6.79 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80-piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5008) shows the static Burn-In circuit. Maxim also performs quarterly 1000-hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The RS29-3 die type has been found to have all pins able to withstand a transient pulse of $\pm 2000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$ and/or $\pm 20\text{V}$.

Table 1
 Reliability Evaluation Test Results
MAX490ExxE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	PDIP	77	0
			NSO	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

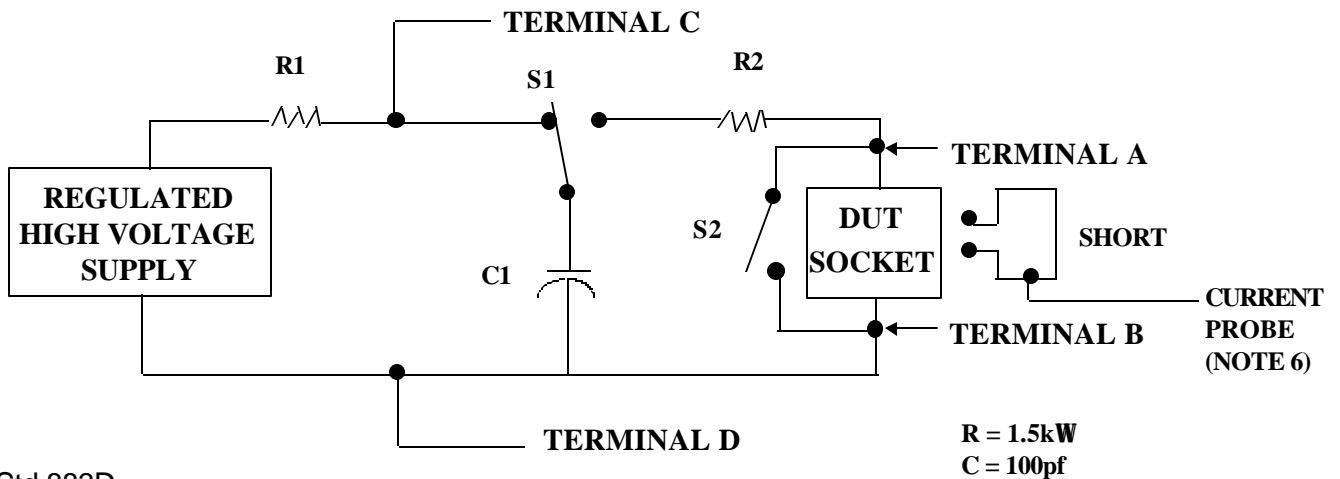
2/ No connects are not to be tested.

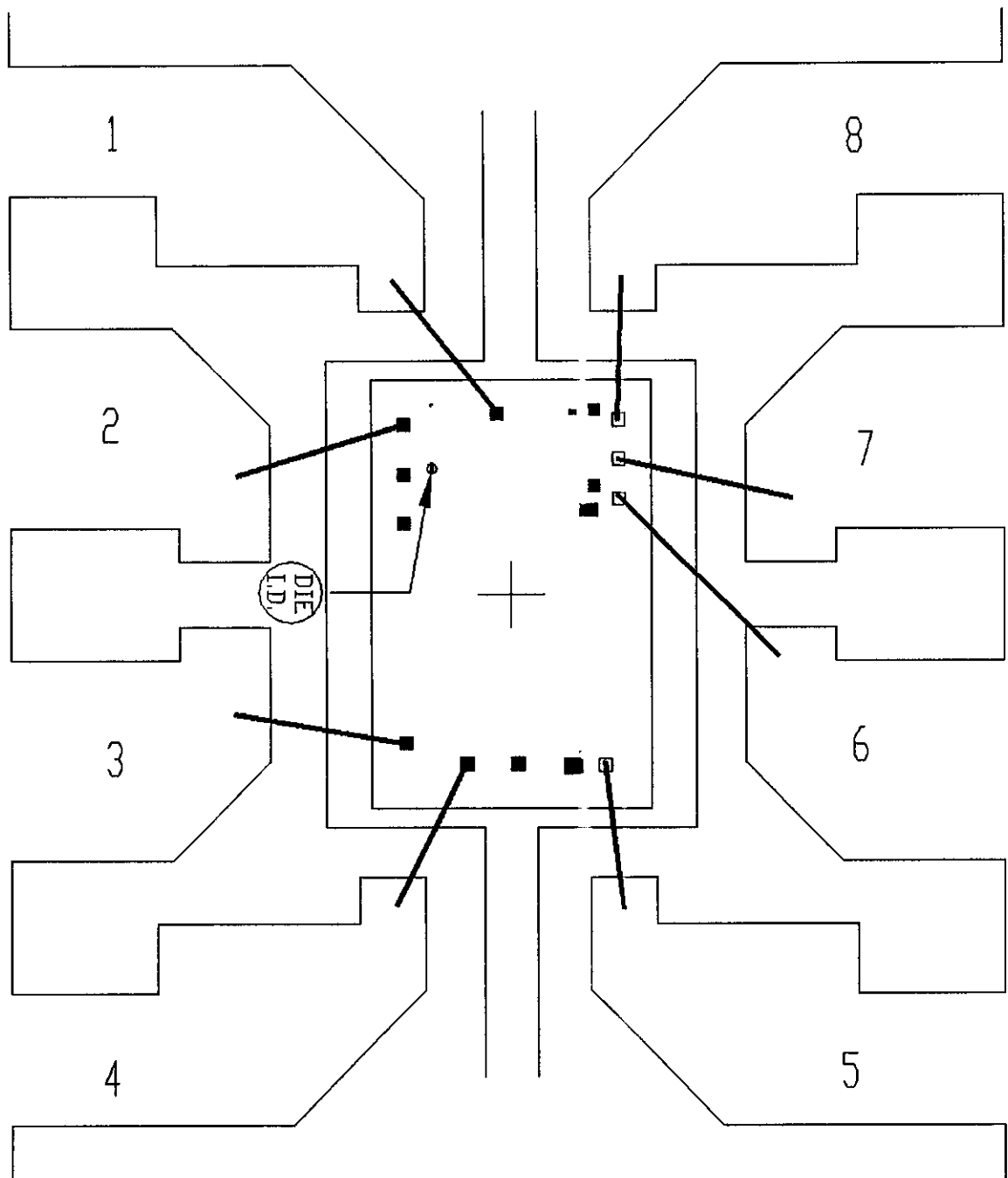
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





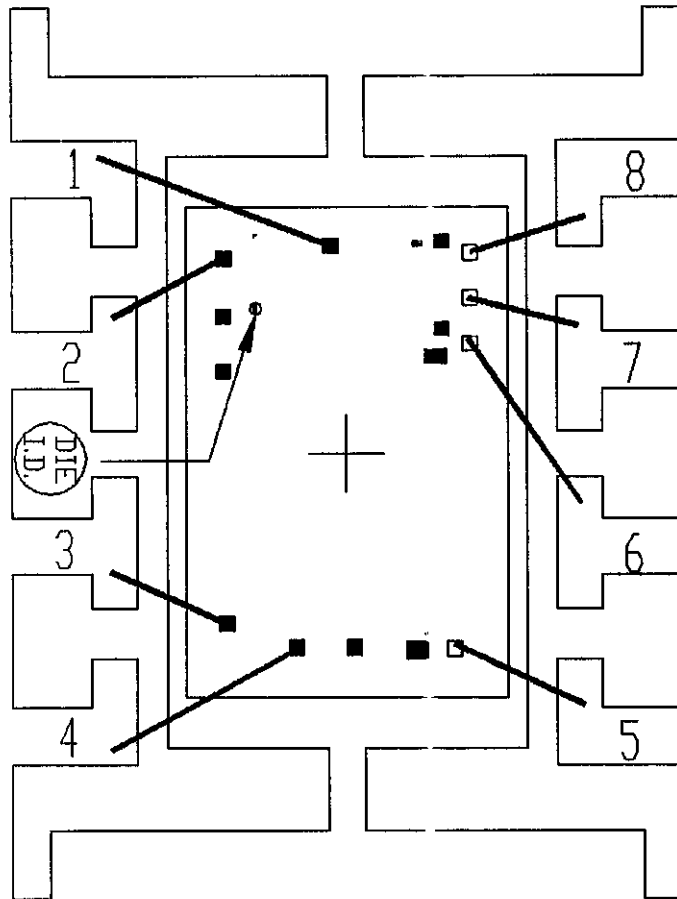
PKG.CODE: P8-2
 CAV./PAD SIZE: 110 X 140

PKG.
 DESIGN

APPROVALS

DATE

MAXIM
 BUILDSHEET NUMBER: 05-1901-0138
 REV.: A



PKG.CODE: S8-5

APPROVALS

DATE



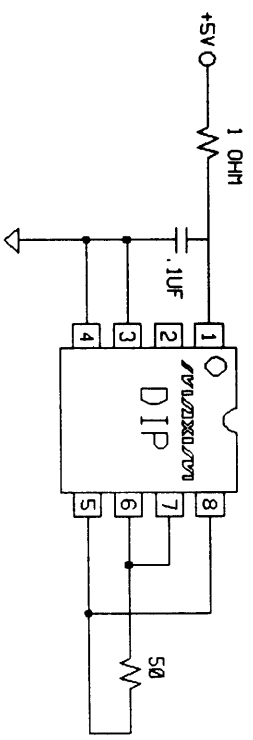
CAV./PAD SIZE:
95 X 155

PKG.
DESIGN

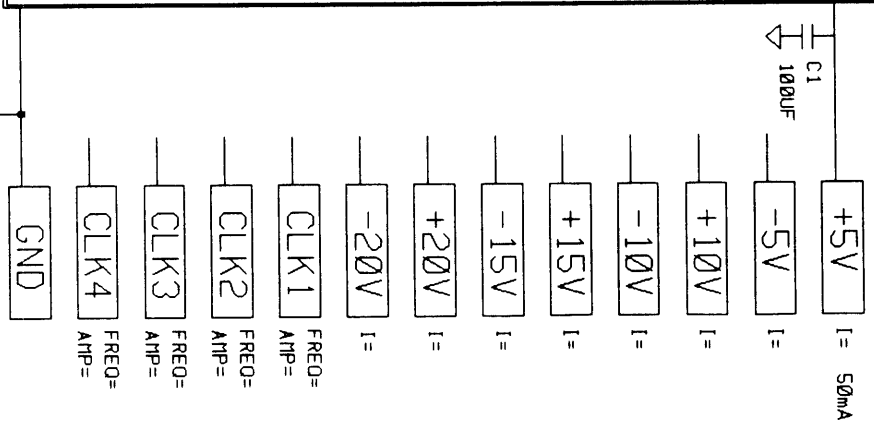
BUILDSHEET NUMBER:
05-1901-0139

REV.:
A

ONCE PER SOCKET



ONCE PER BOARD



- STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
 - BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. C

NOTES :

1. TEMPERATURE : 125C OR EQUIVALENT
2. TIME : 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL [X] HR/883

SPEC. NO. 06-~~S008~~ REV. B

DATE : 7/26/93

DRAWN BY :

MAXIMUM BURN-IN SCHEMATIC

DEVICE TYPE :

MAX488/490