

RELIABILITY REPORT  
FOR  
**MAX4066Axxx**  
PLASTIC ENCAPSULATED DEVICES

July 21, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.  
SUNNYVALE, CA 94086

Written by



Jim Pedicord  
Quality Assurance  
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl  
Quality Assurance  
Executive Director

## Conclusion

The MAX4066A successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents

I. ....Device Description	V. ....Quality Assurance Information
II. ....Manufacturing Information	VI. ....Reliability Evaluation
III. ....Packaging Information	
IV. ....Die Information	.....Attachments

## I. Device Description

### A. General

The MAX4066A quad, SPST, CMOS analog switch is designed to provide superior performance over the industry-standard device. This new switch features guaranteed operation from +2.0V to +16V and is fully specified at 3V, 5V, and 12V. This part offers 45Ω on-resistance and 2Ω channel-to-channel matching at 12V, plus 4Ω flatness over the specified signal range.

The MAX4066A is controlled by TTL/CMOS input levels and can be used as a bilateral switch or multiplexer/demultiplexer.

Low off leakage current (100pA) and low power consumption (0.5μW) make the MAX4066A ideal for battery-operated equipment. This part is also suitable for low-distortion audio applications. ESD protection is greater than 2000V per Method 3015.7.

### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Voltages referenced to GND	
V+	-0.3V to +17V
V <sub>IN</sub> , V <sub>COM</sub> , V <sub>NO</sub> (Note 1)	-0.3V to (V+ + 0.3V)
Current (any terminal)	30mA
Peak Current (any terminal)	100mA
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	762mW
Derates above +70°C	9.52mW/°C
Continuous Power Dissipation (TA = +70°C)	
14-Pin Plastic DIP	800mW
14-Pin Narrow SO	640mW
16-Pin QSOP	762mW
Derates above +70°C	
14-Pin Plastic DIP	10.0mW/°C
14-Pin Narrow SO	8.0mW/°C
16-Pin QSOP	9.52mW/°C

**Note 1:** Signals on NO\_, COM\_, or IN\_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

## II. Manufacturing Information

A. Description/Function:	Low-Cost, Low-Voltage, Quad, SPST, CMOS Analog Switch
B. Process:	SG5 (Standard 5 micron silicon gate CMOS)
C. Number of Device Transistors:	69
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Thailand or Malaysia
F. Date of Initial Production:	September, 1995

## III. Packaging Information

A. Package Type:	<b>14-Lead PDIP</b>	<b>14-Lead NSO</b>	<b>16 Lead QSOP</b>
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0301-0730	# 05-0301-0731	# 05-0301-0732
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1	Level 1	Level 1

## IV. Die Information

A. Dimensions:	65 x 108 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)  
Bryan Preeshl (Executive Director)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

↑  
Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 13.57 \times 10^{-9}$$

$$\lambda = 13.57 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5138) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

### C. E.S.D. and Latch-Up Testing

The AG78 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2500\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX4066Axxx**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test (Note 1)</b>					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
<b>Moisture Testing (Note 2)</b>					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP	77	0
			NSO	77	0
			QSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress (Note 2)</b>					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

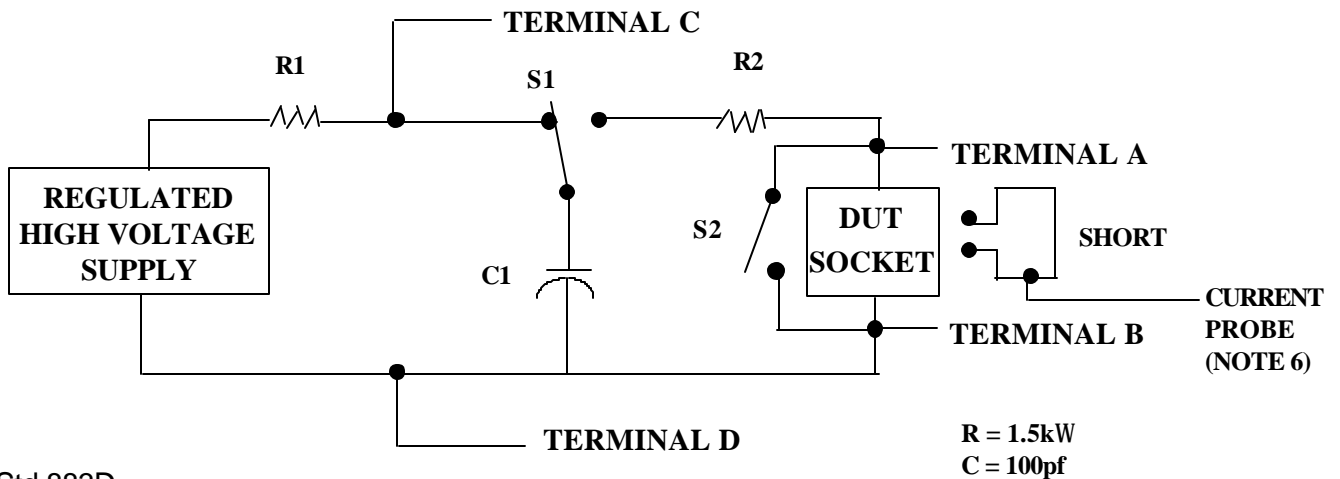
2/ No connects are not to be tested.

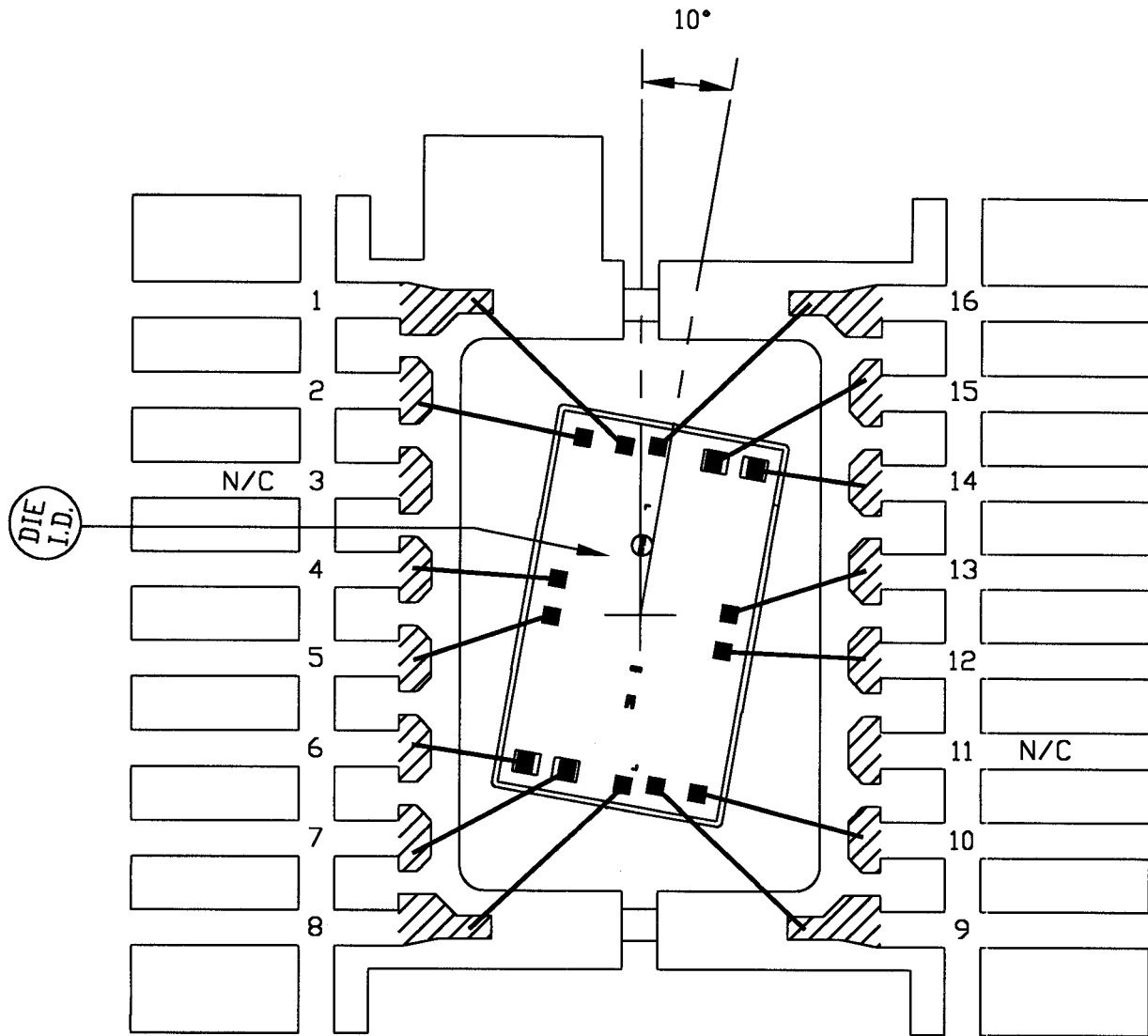
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ ,  $GND$ ,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: E16-5

CAV./PAD SIZE:  
101x154

PKG.  
DESIGN

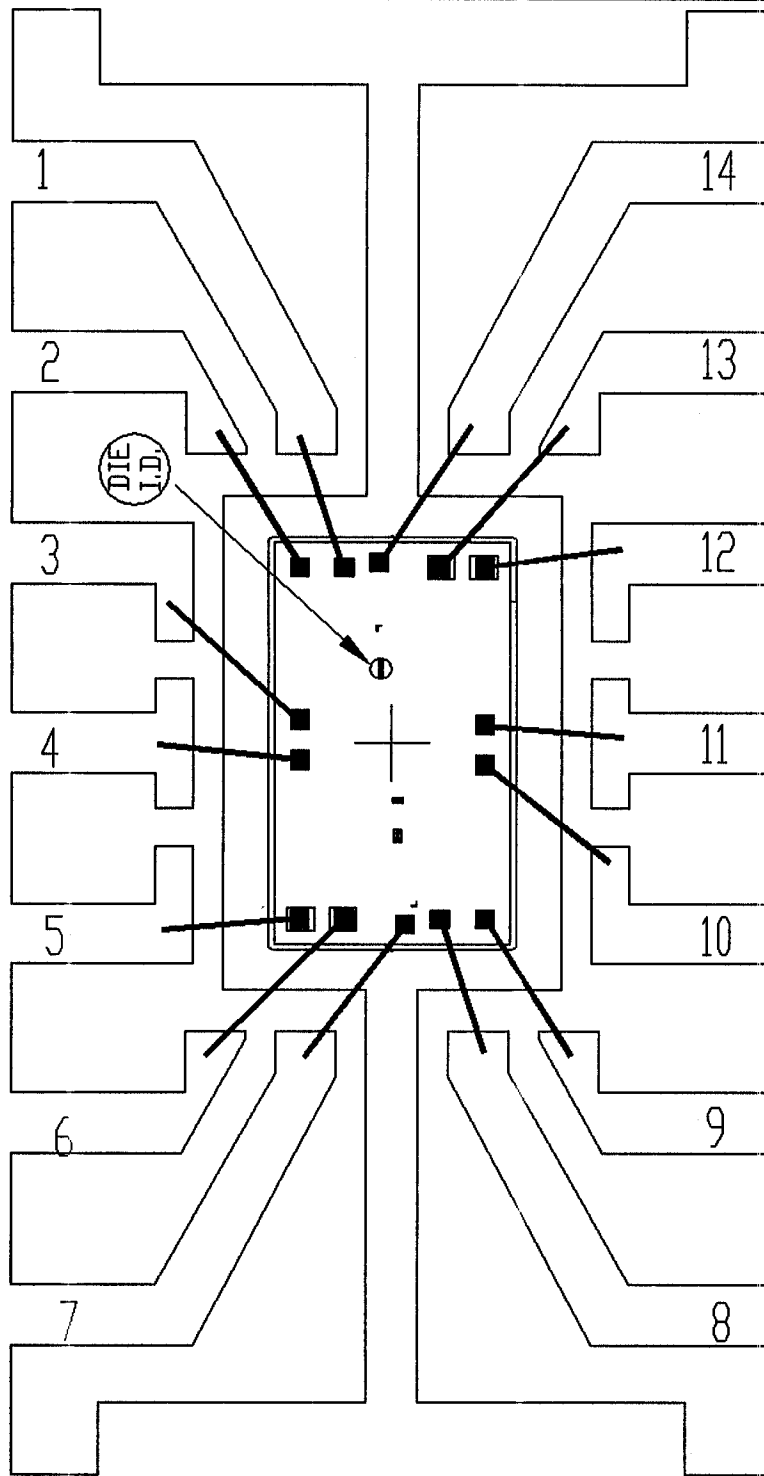
APPROVALS

DATE

**MAXIM**

BUILDSHEET NUMBER:  
05-0301-0732

REV.:  
B



PKG. CODE:	S14-2	
CAV./PAD SIZE:	90 X 130	PKG. DESIGN

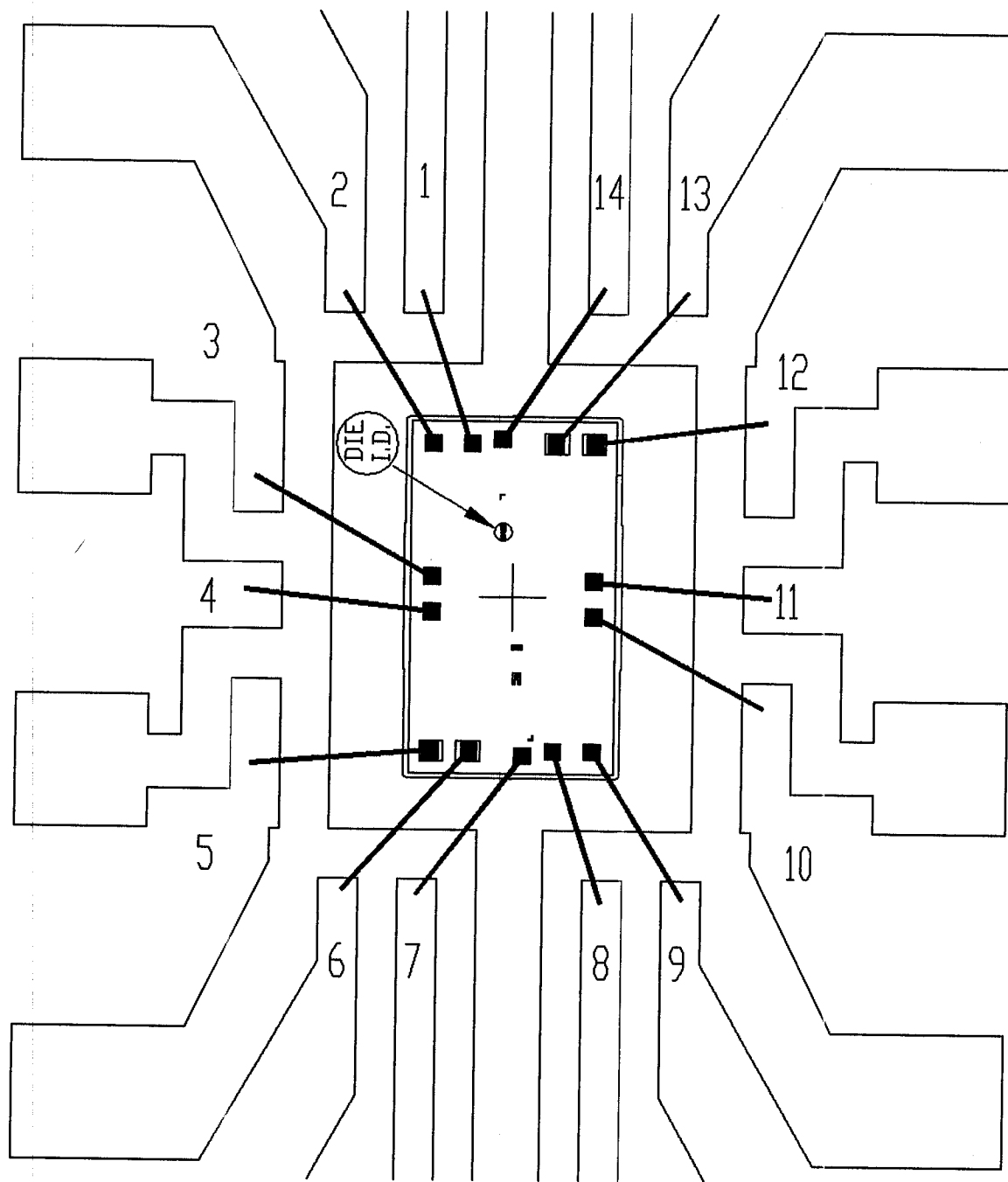
APPROVALS

DATE



BUILD SHEET NUMBER:  
05-0301-0731

REV.:  
A



PKG.CODE: P14-3

CAV./PAD SIZE:  
110 X 140

PKG.  
DESIGN

APPROVALS

DATE

**MAXIM**

BUILDSHEET NUMBER:  
05--0301-0730

REV.:  
A

