

RELIABILITY REPORT  
FOR  
**MAX3748AETE**  
PLASTIC ENCAPSULATED DEVICES

August 1, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord  
Quality Assurance  
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl  
Quality Assurance  
Executive Director

## Conclusion

The MAX3748 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents

I. ....Device Description	V. ....Quality Assurance Information
II. ....Manufacturing Information	VI. ....Reliability Evaluation
III. ....Packaging Information	
IV. ....Die Information	.....Attachments

### I. Device Description

#### A. General

The MAX3748A multirate limiting amplifier functions as a data quantizer for SONET, Fibre Channel, and Gigabit Ethernet optical receivers. The amplifier accepts a wide range of input voltages and provides constant-level current-mode logic (CML) output voltages with controlled edge speeds.

A received-signal-strength indicator (RSSI) is available when the MAX3748A is combined with the MAX3744 SFP transimpedance amplifier (TIA). A receiver consisting of the MAX3744\* and the MAX3748A can provide up to 19dB RSSI dynamic range. Additional features include a programmable loss-of-signal (LOS) detect, an optional disable function (DISABLE), and an output signal polarity reversal (OUTPOL). Output disable can be used to implement squelch.

The combination of the MAX3748A and the MAX3744 allows for the implementation of all the small-form-factor SFF-8472 digital diagnostic specifications using a standard 4-pin TO-46 header. The MAX3748A is packaged in a 3mm x 3mm 16-pin QFN package with an exposed pad.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Power-Supply Voltage (VCC)	-0.5V to +6.0V
Voltage at IN+, IN-	(VCC - 2.4V) to (VCC + 0.5V)
Voltage at DISABLE, OUTPOL, RSSI, CAZ1, CAZ2, LOS, TH	-0.5V to (VCC + 0.5V)
Current into LOS	-1mA to +9mA
Differential Input Voltage (IN+ - IN-)	2.5V
Continuous Current at CML Outputs (OUT+, OUT-)	-25mA to +25mA
Operating Junction Temperature Range (TJ)	-55°C to +150°C
Storage Ambient Temperature Range (Ts)	-55°C to +150°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin QFN (3x3)	1400mW
Derates above +70°C	
16-Pin QFN (3x3)	17.7mW/°C

## II. Manufacturing Information

A. Description/Function:	Compact 155Mbps to 3.2Gbps Limiting Amplifier
B. Process:	GST4-F60
C. Number of Device Transistors:	1468
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia
F. Date of Initial Production:	January, 2003

## III. Packaging Information

A. Package Type:	<b>16-Pin Thin QFN (3x3) Flip Chip</b>
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	N/A
E. Bondwire:	5 mil dia. ball
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-0299
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

## IV. Die Information

A. Dimensions:	84 x 84 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1: 1.2; Metal2: 1.2; Metal3: 1.2; Metal4: 5.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1: 1.6; Metal2: 1.6; Metal3: 1.6; Metal4: 4.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 9823 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 10.78 \times 10^{-8} \quad \lambda = 10.78 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-7099) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Reports (**RR-1M & RR-B3A**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The HD41-1 die type has been found to have all pins able to withstand a transient pulse of +/-2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX3748AETE**

<b>TEST ITEM</b>	<b>TEST CONDITION</b>	<b>FAILURE IDENTIFICATION</b>	<b>SAMPLE SIZE</b>	<b>NUMBER OF FAILURES</b>
<b>Static Life Test</b> (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
<b>Moisture Testing</b> (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
<b>Mechanical Stress</b> (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

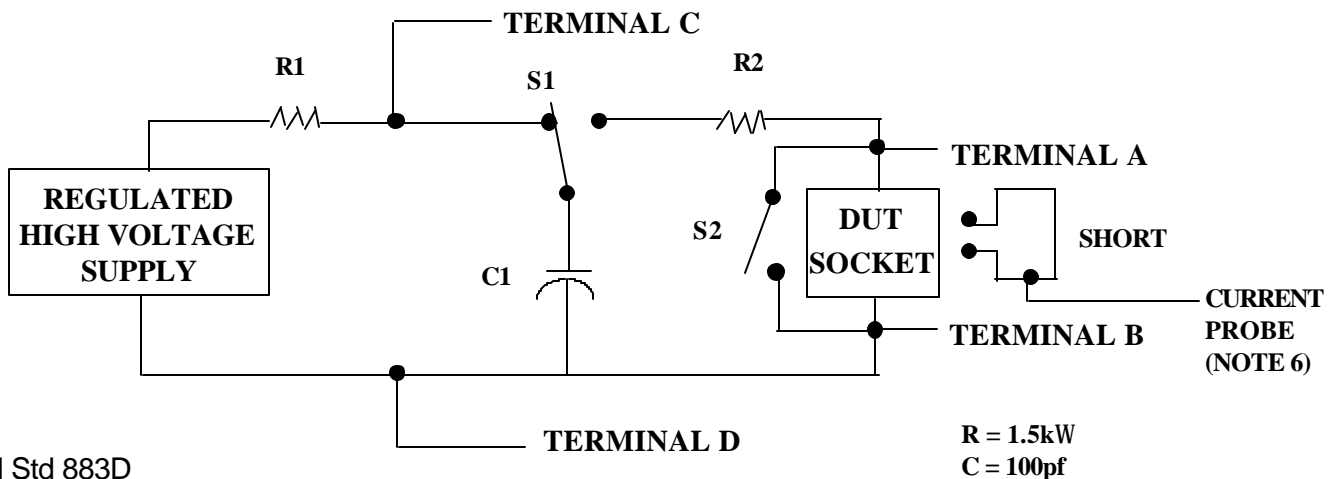
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

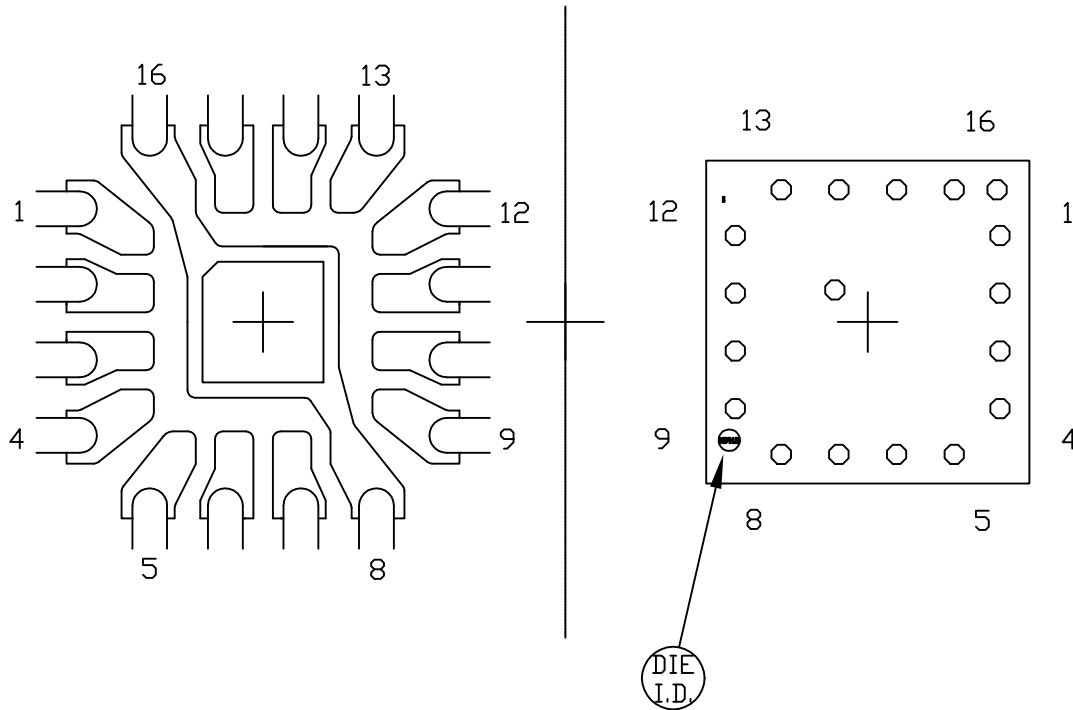
3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



3x3x0.8mm QFN THIN PKG.  
 FLIP CHIP  
 WITH EXPOSED PAD

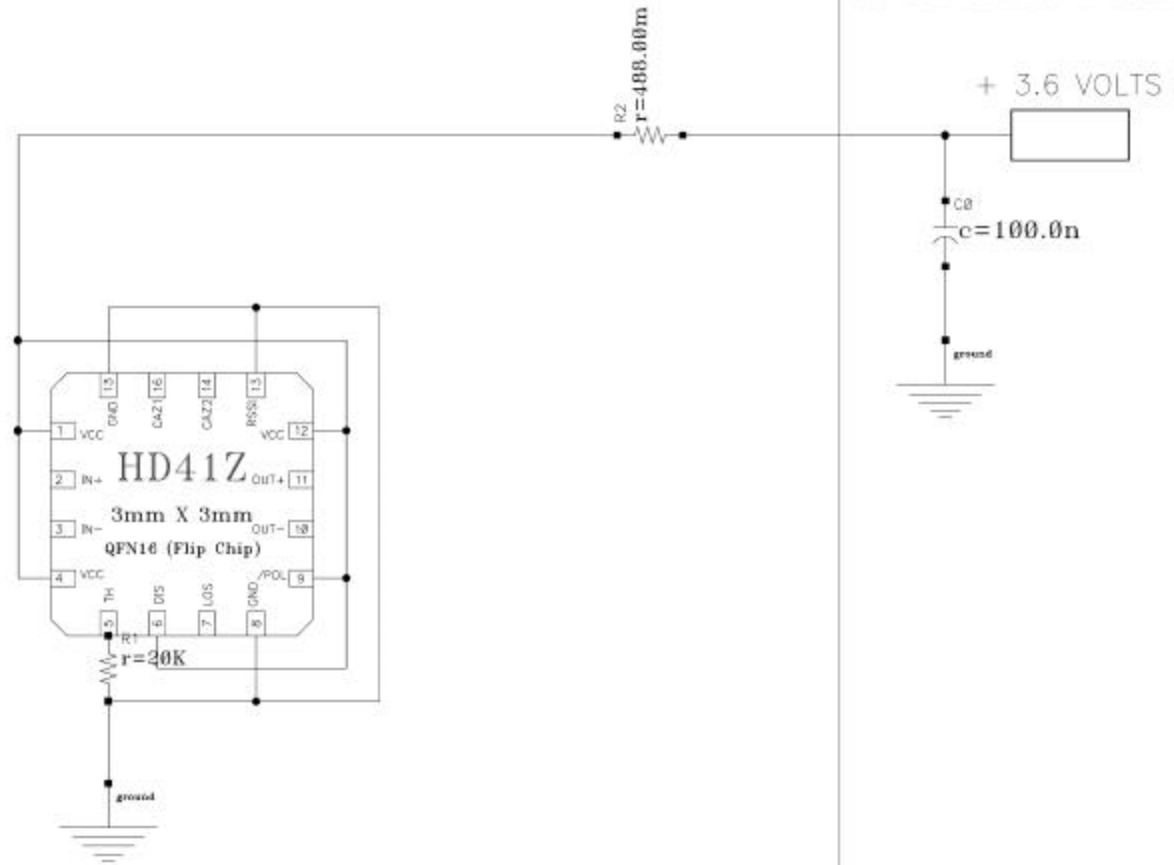
FLIP LINE



PKG. CODE: T1633F-3		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: FLIP CHIP	PKG. DESIGN			BOND DIAGRAM #: 05-9000-0299	REV: A

ONCE PER SOCKET

ONCE PER BOARD



HEADER GROUNDED (Yes/No):

PRODUCT: MAX3748 PACKAGE TYPE: QFN16(FC)  
 VERSION #: (Daughter Card) DATE : Aug 6 11:51:04 2002  
 ICC (MAX) : 73.7 mA  
 VCC : 3.6 VOLTS

NOTES: DIE TYPE = HD41Z