

RELIABILITY REPORT
FOR
MAX3746ETE
PLASTIC ENCAPSULATED DEVICES

February 2, 2010

MAXIM INTEGRATED PRODUCTS

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Approved by
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Conclusion

The MAX3746ETE successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX3746 multirate limiting amplifier functions as a data quantizer for SONET, Fibre-Channel, and Gigabit Ethernet optical receivers. The amplifier accepts a wide range of input voltages and provides selectable-level, current-mode logic (CML) output voltages with controlled edge speeds. A received-signal-strength indicator (RSSI) is available when the MAX3746 is DC-coupled to the MAX3744/MAX3724 SFP transimpedance amplifier (TIA). A receiver consisting of the MAX3744/MAX3724 and the MAX3746 can provide up to 19dB RSSI dynamic range. Additional features include a programmable loss-of-signal (LOS) detect, an optional disable function (DISABLE), and an output-signal polarity reversal (OUTPOL). Output disable can be used to implement squelch. The combination of the MAX3746 and the MAX3744/MAX3724 allows for the implementation of all the small-form-factor SFF-8472 digital diagnostic specifications using a standard 4-pin TO-46 header. The MAX3746 is pin-for-pin compatible with the MAX3748A limiting amplifier and consumes 30% less power. The MAX3746 is packaged in a 3mm x 3mm, 16-pin QFN package.

II. Manufacturing Information

A. Description/Function:	Low-Power, 622Mbps to 3.2Gbps Limiting Amplifier
B. Process:	G4
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Malaysia, Thailand
F. Date of Initial Production:	July 09, 2004

III. Packaging Information

A. Package Type:	16-pin TQFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	85Sn/15Pb plate
D. Die Attach:	None
E. Bondwire:	Au (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0768
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	64°C/W
K. Multi Layer Theta Ja:	57.2°C/W
L. Multi Layer Theta Jc:	40°C/W

IV. Die Information

A. Dimensions:	83 X 83 mils
B. Passivation:	Si ₃ N ₄
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 23.9 \times 10^{-9}$$
$$\lambda = 23.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the G4 Process results in a FIT Rate of 0.02 @ 25C and 0.37 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The HD50 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX3746ETE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data