

RELIABILITY REPORT
FOR
MAX3232xxE+
PLASTIC ENCAPSULATED DEVICES

11/3/08

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Ken Wendel
Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX3232 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX3232 transceiver has a proprietary low-dropout transmitter output stage enabling true RS-232 performance from a 3.0V to 5.5V supply with a dual charge pump. This device requires only four small 0.1 μ F external charge-pump capacitors. The MAX3232 is guaranteed to run at data rates of 120kbps while maintaining RS-232 output levels.

This device has 2 receivers and 2 drivers. The MAX3232 is pin, package, and functionally compatible with the industry-standard MAX232.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
V _{CC}	-0.3V to +6V
V ₊ (Note 1)	-0.3V to +7V
V ₋ (Note 1)	+0.3V to -7V
V ₊ + V ₋ (Note 1)	+13V
Input Voltages	
T _{IN} , /SHDN, /EN	-0.3V to +6V
MBAUD	-0.3V to (V _{CC} + 0.3V)
R _{IN}	±25V
Output Voltages	
T _{OUT}	±13.2V
R _{OUT}	-0.3V to (V _{CC} + 0.3V)
Short-Circuit Duration	
T _{OUT}	Continuous
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
16-Pin DIP	842mW
16-Pin NSO	696mW
16-Pin WSO	762mW
16-Pin TSSOP	533mW
Derates above +70°C	
16-Pin DIP	10.53mW/°C
16-Pin NSO	8.70mW/°C
16-Pin WSO	9.52mW/°C
16-Pin TSSOP	6.70mW/°C

Note 1: V₊ and V₋ can have a maximum magnitude of 7V, but their absolute difference cannot exceed 13V.

II. Manufacturing Information

- A. Description/Function: 3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceiver Using Four 0.1 μ F External Capacitors
- B. Process: S3 (Standard 3 micron silicon gate CMOS)
- C. Number of Device Transistors: 339
- D. Fabrication Location: Oregon, USA
- E. Assembly Location: Philippines, Malaysia, Korea, or Thailand
- F. Date of Initial Production: October, 1994

III. Packaging Information

- | A. Package Type: | 16-Pin PDIP | 16-Pin WSO | 16-Pin NSO | 16-Pin TSSOP |
|--|-------------------------------|--------------------------|--------------------------|------------------------|
| B. Lead Frame: | Copper | Copper | Copper | Copper |
| C. Lead Finish: | 100% Matte Tin (all packages) | | | |
| D. Die Attach: | Silver-filled Epoxy | Silver-filled Epoxy | Silver-filled Epoxy | Silver-filled Epoxy |
| E. Bondwire: | Gold (1.3 mil dia.) | Gold (1.3 mil dia.) | Gold (1.3 mil dia.) | Gold (1.3 mil dia.) |
| F. Mold Material: | Epoxy with silica filler | Epoxy with silica filler | Epoxy with silica filler | Epoxy w/ silica filler |
| G. Assembly Diagram: | # 05-1901-0246 | # 05-1901-0255 | # 05-1901-0249 | # 05-1901-0262 |
| H. Flammability Rating: | Class UL94-V0 | Class UL94-V0 | Class UL94-V0 | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-022C: | Level 1 (all package styles) | | | |

IV. Die Information

- A. Dimensions: 123 x 87 mils
- B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 3 microns (as drawn)
- F. Minimum Metal Spacing: 3 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric: SiO₂
- I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 520 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 2.09 \times 10^{-9} \quad \lambda = 2.09 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at <http://www.maxim-ic.com/>. Current monitor data for the S3 Process results in a FIT Rate of 3.6 @ 25C and 66.0 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The RS21 die type has been found to have all pins able to withstand a transient pulse of $\pm 2500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$ and/or $\pm 20\text{V}$.

Table 1
Reliability Evaluation Test Results

MAX3223xxE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		520	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP	77	0
			NSO	77	0
			TSSOP	77	0
			WSO	77	2
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic Package/Process data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

2/ No connects are not to be tested.

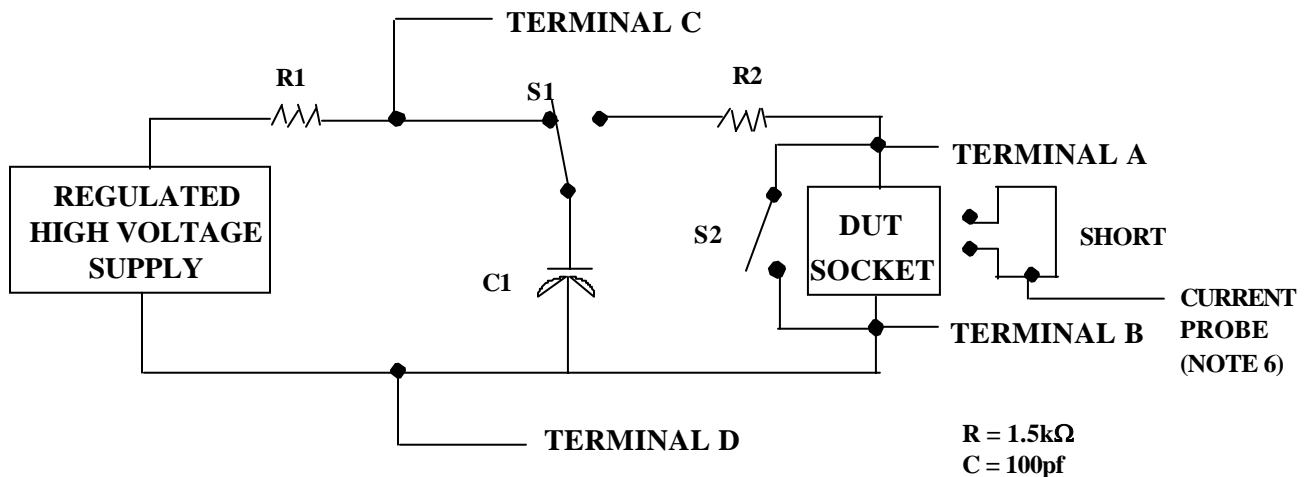
3/ Repeat pin combination I for each named Power supply and for ground

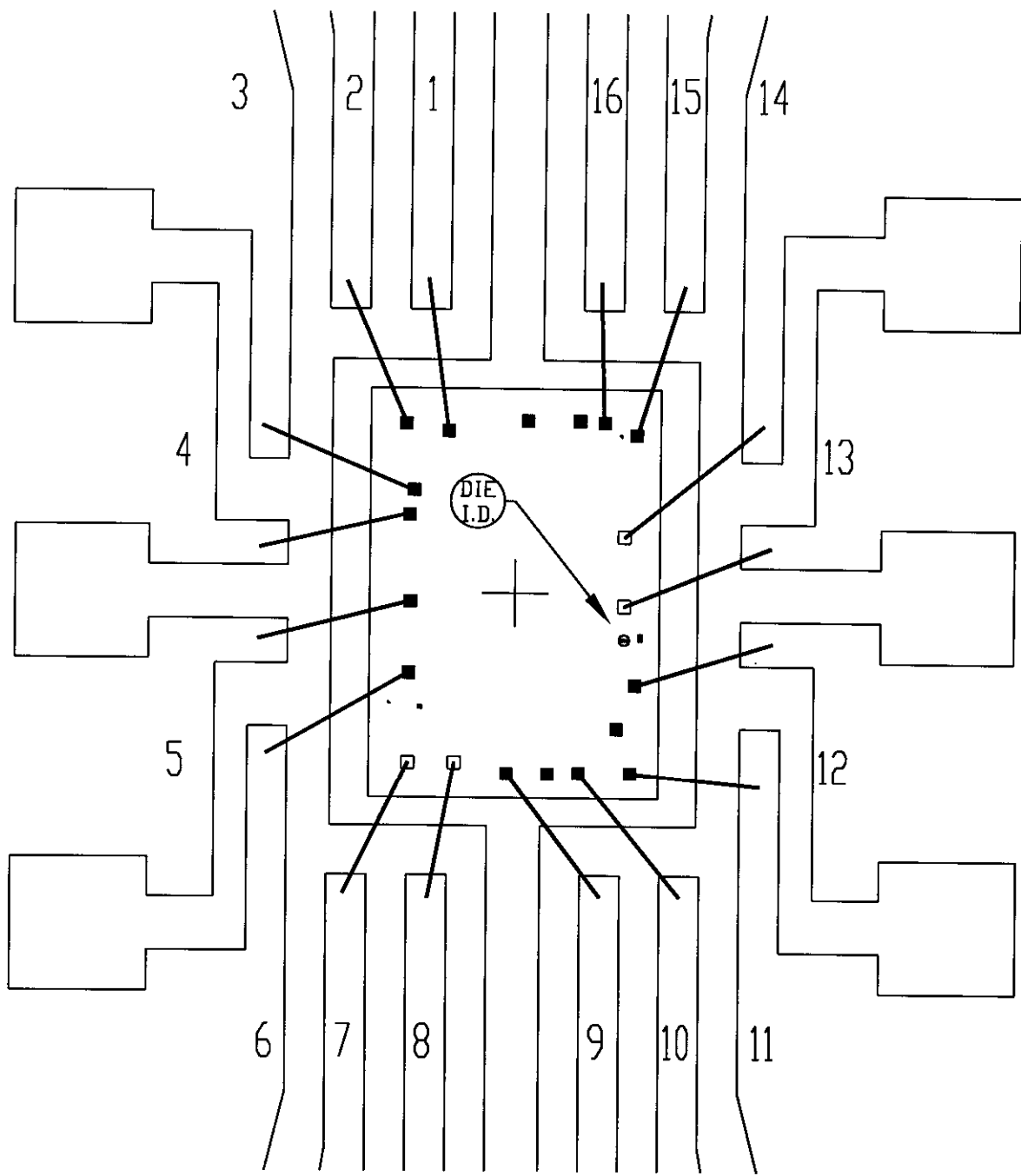
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).


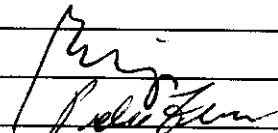
3.4 Pin combinations to be tested.

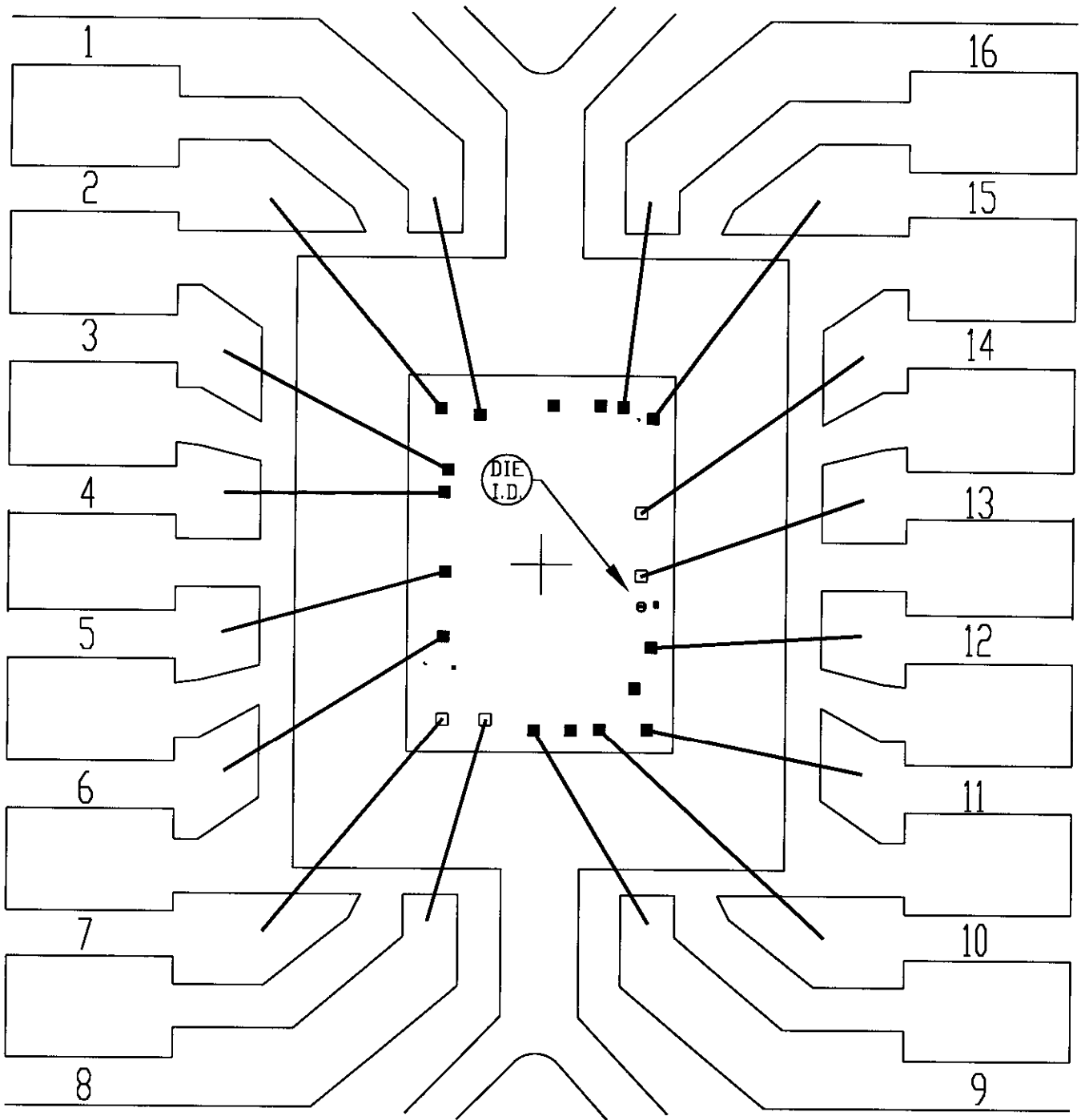
- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.


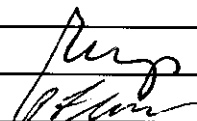
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

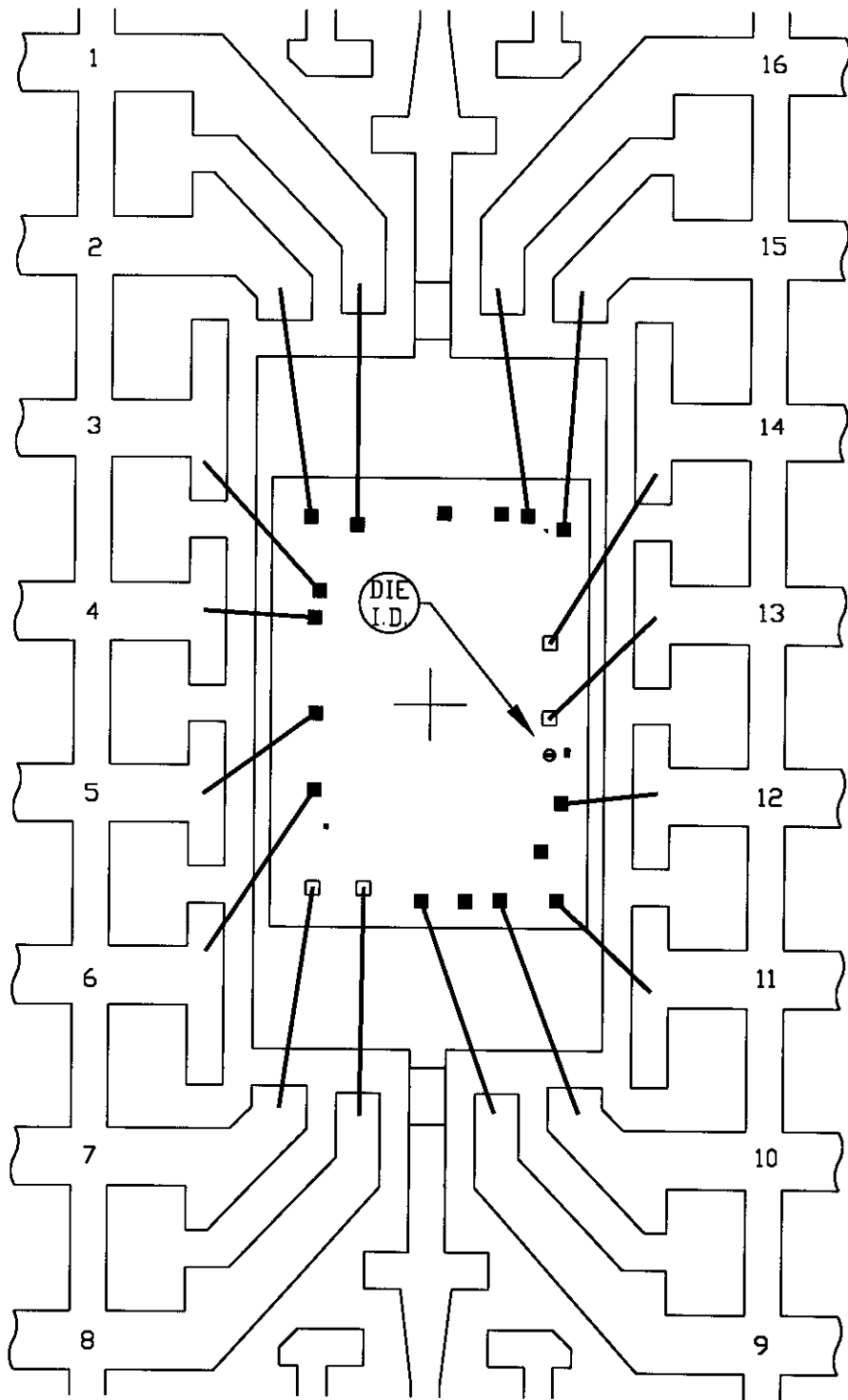



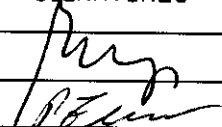


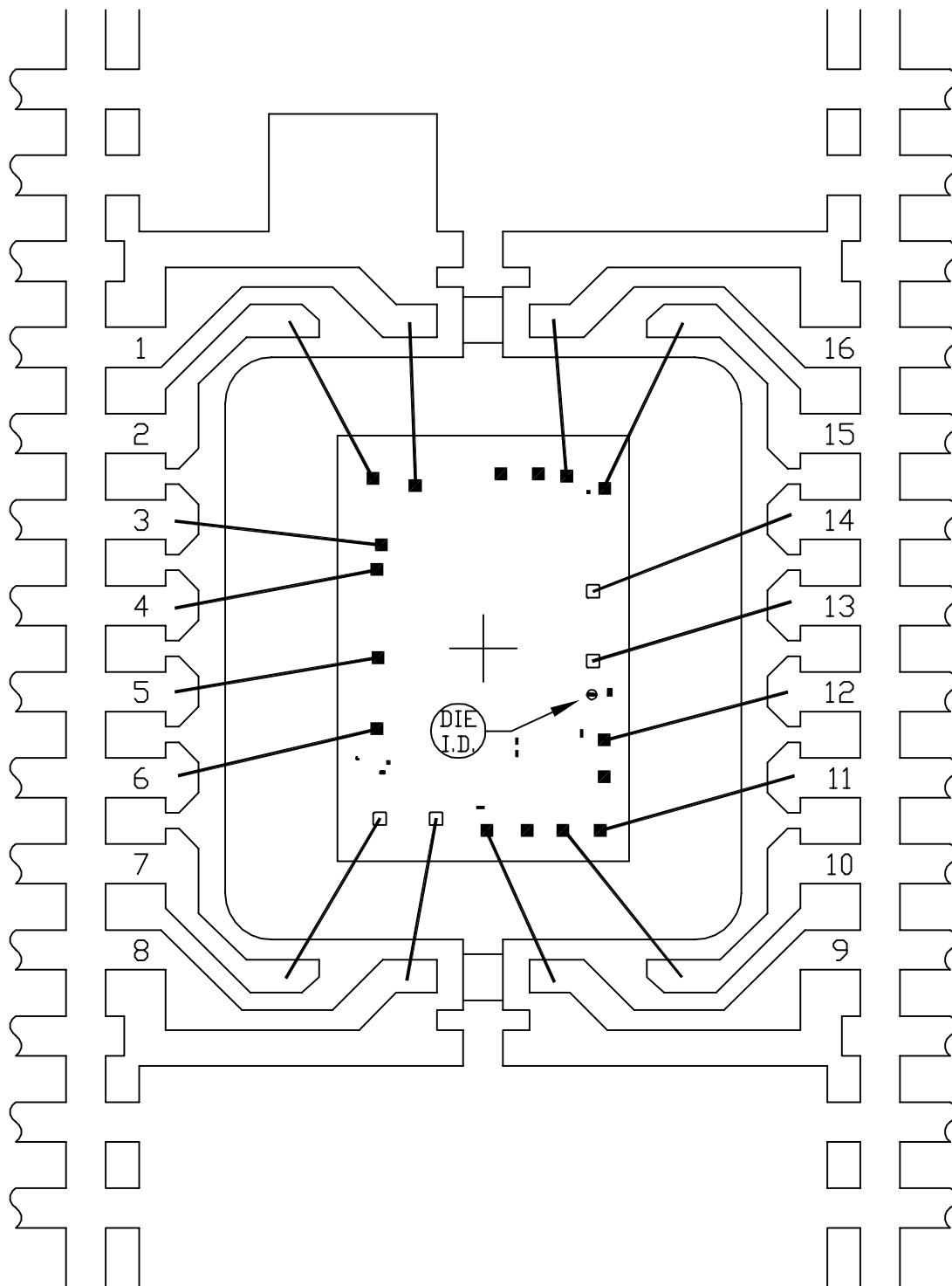
PKG. CODE: P16-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 110x140	PKG.		8/21/00	BOND DIAGRAM #:	REV:
	DESIGN		8-22-00	05-1901-0246	A



PKG. CODE: W16-3		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 160 X 200	PKG. DESIGN		8/21/00	BOND DIAGRAM #:	REV:
			8-22-00	05-1901-0255	A



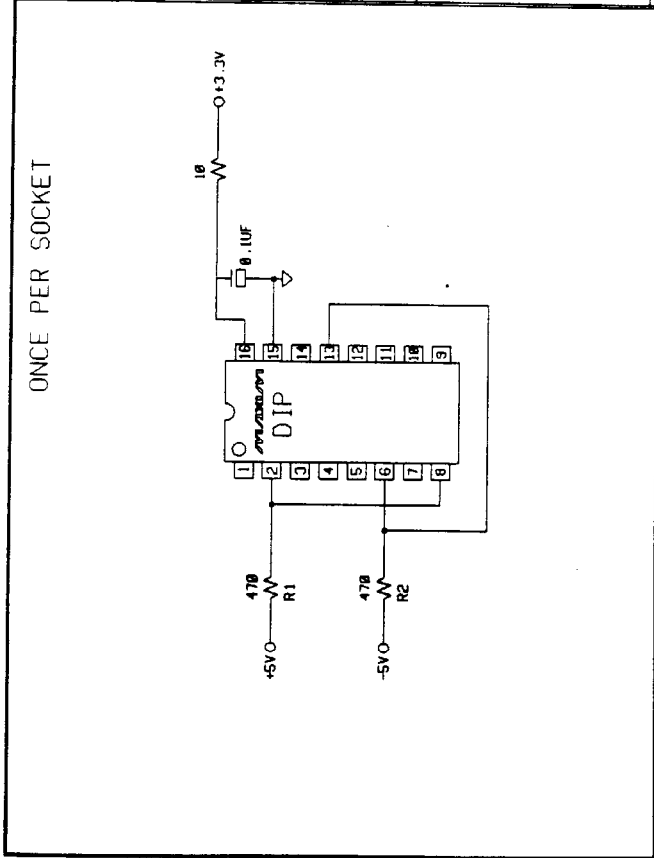
PKG. CODE: S16-5		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 96X190	PKG.		8/21/00	BOND DIAGRAM #:	REV:
	DESIGN		8-22-00	05-1901-0249	A



PKG. CODE: A16-2		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 154X173	PKG. DESIGN			BOND DIAGRAM #: 05-1901-0262	REV: A

ONCE PER BOARD

ONCE PER SOCKET



—STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
 —BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 168 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL [X] HR/883

SPEC. NO. 06-5054 REV. C

DATE: 11/11/99

DRAWN BY: T. BEJSOVEC

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE:

MAX3232/E

MAX 3316 E

