MAX2015EUA
Rev. A

RELIABILITY REPORT

FOR

MAX2015EUA

PLASTIC ENCAPSULATED DEVICES

February 10, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX2015 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX2015 complete multistage logarithmic amplifier is designed to accurately convert radio-frequency (RF) signal power in the 0.1GHz to 2.5GHz frequency range to an equivalent DC voltage. The outstanding dynamic range and precision over temperature of this log amplifier make it particularly useful for a variety of base station and other wireless applications, including automatic gain control (AGC), transmitter power measurements, and received signal strength indication (RSSI) for terminal devices.

The MAX2015 can also be operated in a controller mode where it measures, compares, and controls the output power of a variable-gain amplifier as part of a fully integrated AGC loop.

This logarithmic amplifier provides much wider measurement range and superior accuracy compared to controllers based on diode detectors, while achieving excellent temperature stability over the full -40°C to +85°C operating range.

B. Absolute Maximum Ratings

Item	Rating
VCC (Pins, 1, 4) to GND	-0.3V to +5.25V
SET, PWDN to GND	-0.3V to (VCC + 0.3V)
Input Power Differential INHI, INLO	+23dBm
Input Power Single Ended (INHI or INLO grounded)	+19dBm
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
8-Pin µMAX	362mW
Derates above +70°C	
8-Pin µMAX	4.5mW/°C

II. Manufacturing Information

A. Description/Function: 0.1GHz to 2.5GHz, 75dB Logarithmic Detector/Controller

B. Process: GST4-MB20 Bi-CMOS Process

C. Number of Device Transistors: 3157

D. Fabrication Location: Oregon, USA

E. Assembly Location: Malaysia, Philippines or Thailand

F. Date of Initial Production: October, 2003

III. Packaging Information

A. Package Type: **8-Pin uMAX**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-Filled Epoxy

E. Bondwire: Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-9000-0692

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 63 x 84 mils

B. Passivation: Si_3N_4 (Silicon nitride)

C. Interconnect: Au

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4

F. Minimum Metal Spacing: 1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4

G. Bondpad Dimensions: 3.4 mil. Octagonal

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 45 \times 2}$$ (Chi square value for MTTF upper limit)

(45:) Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 10.78 \times 10^{-9}$ λ = 10.78 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic #06-7100 shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-B2A**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The CR11 die type has been found to have all pins able to withstand a transient pulse of +/-1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit).

Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX2015EUA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification packages.
Note 2: Generic package/process data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

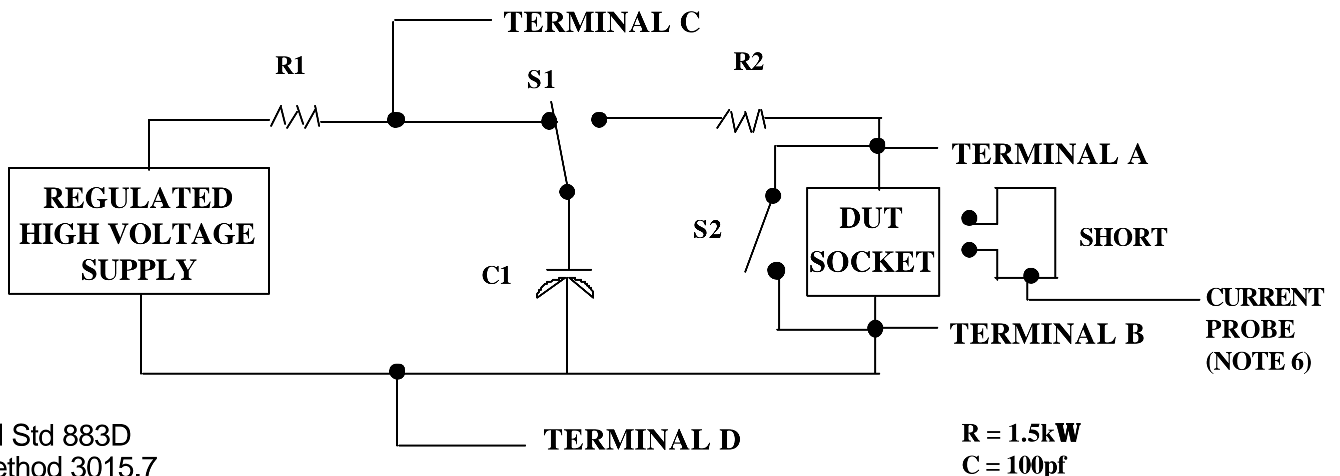
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

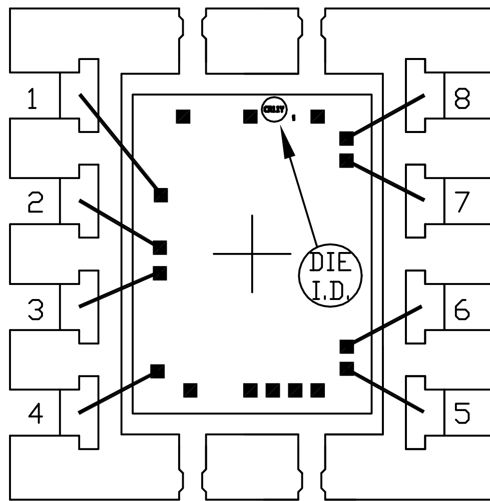
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

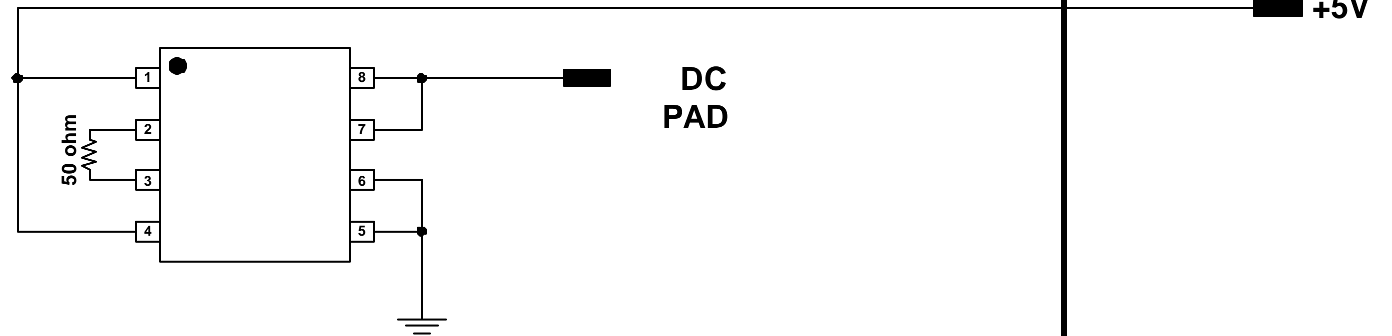




PKG. CODE: U8-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 68x94	PKG.			BOND DIAGRAM #: 05-9000-0692	REV: A
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 2015
PACKAGE: 8-Umax
MAX. EXPECTED CURRENT = 20mA

DRAWN BY: HAK TAN
NOTES: DC pad is a monitor pin at each socket to measure current to device and DC voltage to determine failure.