

RELIABILITY REPORT  
FOR  
**MAX1946ETA**  
PLASTIC ENCAPSULATED DEVICES

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**MAXIM INTEGRATED PRODUCTS**

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## Conclusion

The MAX1946 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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## I. Device Description

### A. General

The MAX1946 single current-limited switch with auto-reset supplies a guaranteed 500mA load in accordance with USB specifications. The MAX1946 operates from a 2.7V to 5.5V input supply and consumes only 40 $\mu$ A of quiescent current when operating and only 3 $\mu$ A in shutdown. Selectable active-high/active-low control logic and shutdown control provide additional flexibility. An autoreset feature latches the switch off in the event of a short circuit, saving system power. The switch reactivates upon removal of the shorted condition.

The MAX1946 provides several safety features to protect the USB port. Built-in thermal-overload protection turns off the switch when the die temperature exceeds +160°C. Accurate internal current-limiting circuitry protects the input supply against both overload and short-circuit conditions. An open-drain fault signal, (FAULT-bar), notifies the microprocessor ( $\mu$ P) when a thermal overload, current-limit, undervoltage lockout (UVLO), or short-circuit fault occurs. A 20ms fault-blanking feature enables the circuit to ignore momentary faults, such as those caused when hot-swapping a capacitive load, preventing false alarms to the host system. The fault-blanking feature prevents fault signals from being issued when the device powers up the load.

The MAX1946 is available in a space-saving 8-pin thin QFN package and operates over the extended (-40°C to +85°C) temperature range.

### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
IN, ON, OUT, SEL to GND	-0.3V to +6V
FAULT to GND	-0.3V to (VIN + 0.3V)
IN to OUT	-0.3V to +6V
OUT Continuous Switch Current (internally limited)	1.3A
FAULT DC Current	10mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)(note 1)	
8-Pin QFN	1951mW
Derates above +70°C	
8-Pin QFN	24.4mW/°C

Note 1- Exposed Pad Must be Soldered to PC Board

## II. Manufacturing Information

A. Description/Function:	Single USB Switch with Autoreset and Fault Blanking in Tiny QFN
B. Process:	B8/S8 - Standard 8 micron silicon gate CMOS
C. Number of Device Transistors:	2004
D. Fabrication Location:	Dallas or California, USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	July, 2002

## III. Packaging Information

A. Package Type:	<b>8-Lead QFN</b>
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-9000-0015
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

## IV. Die Information

A. Dimensions:	44 X 82 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	TiW/ AlCu/ TiWN
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)  
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 187 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

△ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 12.93 \times 10^{-9} \quad \lambda = 12.93 \text{F.I.T. (60\% confidence level @ 25°C)}$$

Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Reliability Monitor Report located on the Maxim website at <http://www.maxim-ic.com>. Current monitor data for the B8/S8 Process results in a FIT Rate of 0.27 @ 25C and 4.64 @ 55C (0.8 eV, 60% UCL)

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The PM73 die type has been found to have all pins able to withstand a transient pulse of  $\pm 800\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX1946ETA**

<b>TEST ITEM</b>	<b>TEST CONDITION</b>	<b>FAILURE IDENTIFICATION</b>	<b>SAMPLE SIZE</b>	<b>NUMBER OF FAILURES</b>
<b>Static Life Test (Note 1)</b>				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	84	0
<b>Moisture Testing (Note 2)</b>				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
<b>Mechanical Stress (Note 2)</b>				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic process/package data

## Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

### 3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

