

RELIABILITY REPORT
FOR
MAX1907AETL
PLASTIC ENCAPSULATED DEVICES

January 12, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
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Written by

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Conclusion

The MAX1907A successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

The MAX1907A is a single-phase, Quick-PWM™ master controllers for IMVP-IV™ CPU core supplies. Multi-phase operation is achieved using a Quick-PWM slave controller (MAX1980). Multiphase operation reduces input ripple current requirements and output voltage ripple while easing component selection and layout difficulties. The MAX1907A includes active voltage positioning with adjustable gain and offset, reducing power dissipation and bulk output capacitance requirements.

The MAX1907A is intended for two different notebook CPU core applications: either bucking down the battery directly, or 5V system supply to create the core voltage. The single-stage conversion method allows these devices to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, two-stage conversion (stepping down the 5V system supply instead of the battery) at higher switching frequency provides the minimum possible physical size.

The MAX1907A meets the IMVP-IV specifications and include logic to interface with the CPU power good signals from the VCCP and VCCMCH rails within the system. The regulator features power-up sequencing, automatically ramping up to the Intel-specified boot voltage. The MAX1907A features independent four-level logic inputs for setting the boot voltage (B0–B2) and the suspend voltage (S0–S2).

The MAX1907A includes output undervoltage protection, thermal protection, and system power-OK (SYSPOK) input/output. When any of these protection features detect a fault, the MAX1907A immediately shuts down. Additionally, the MAX1907A includes overvoltage protection.

The MAX1907A is available in a thin 40-pinQFN package.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
V+ to GND	-0.3V to +30V
VCC, VDD to GND	-0.3V to +6V
SYSPOK, IMVPOK, CLKEN to GND	-0.3V to +6V
DPSLP, SUS, D0–D5 to GND	-0.3V to +6V
REF, ILIM, CSP, CSN to GND.....	-0.3V to (VCC + 0.3V)
FB, POS, NEG, OAIN+, CC	
OAIN- to GND.....	-0.3V to (VCC + 0.3V)
B0–B2, S0–S2, TON,	
TIME to GND	-0.3V to (VCC + 0.3V)
DL, DDO, to PGND.....	-0.3V to (VDD + 0.3V)
DH to LX.....	-0.3V to (VBST + 0.3V)
SHDN to GND.....	-0.3 to +18V
BST to GND	-0.3 to +36V
LX to BST.....	-6V to +0.3V
GND to PGND	-0.3V to +0.3V
REF Short-Circuit Duration	Continuous
Continuous Power Dissipation	
40-Pin 6mm × 6mm Thin QFN	
(derate 26.3mW/°C above +70°C).....	2105mW
Operating Temperature Range	-40°C to +100°C
Junction Temperature.....	+150°C
Storage Temperature.....	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

- A. Description/Function: Quick-PWM Master Controllers for Voltage- Positioned CPU Core Power Supplies (IMVP-IV)
- B. Process: B12 (Standard 1.2 micron silicon gate CMOS)
- C. Number of Device Transistors: 8713
- D. Fabrication Location: California, USA
- E. Assembly Location: Thailand or Hong King
- F. Date of Initial Production: April, 2002

III. Packaging Information

- A. Package Type: **40-Lead Thin QFN (6x6)**
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate or 100% Matte Tin
- D. Die Attach: Silver-filled epoxy
- E. Bondwire: Gold (1.3 mil dia)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: Buildsheet # 05-3801-0013
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity
Per JEDEC standard J-STD-020-C: Level 1

IV. Die Information

- A. Dimensions: 130 x 131 mils
- B. Passivation: $\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Copper/Silicon
- D. Backside Metallization: None
- E. Minimum Metal Width: 1.2 microns (as drawn)
- F. Minimum Metal Spacing: 1.2 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric: SiO_2
- I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 89 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

↳ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 12.35 \times 10^{-9} \quad \lambda = 12.35 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5973) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B12/S12 Process results in a FIT rate of 0.10 @ 25°C and 1.73 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PD26 die type has been found to have all pins able to withstand a transient pulse of $\pm 1500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX1907AETL

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		89	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic package/process data

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

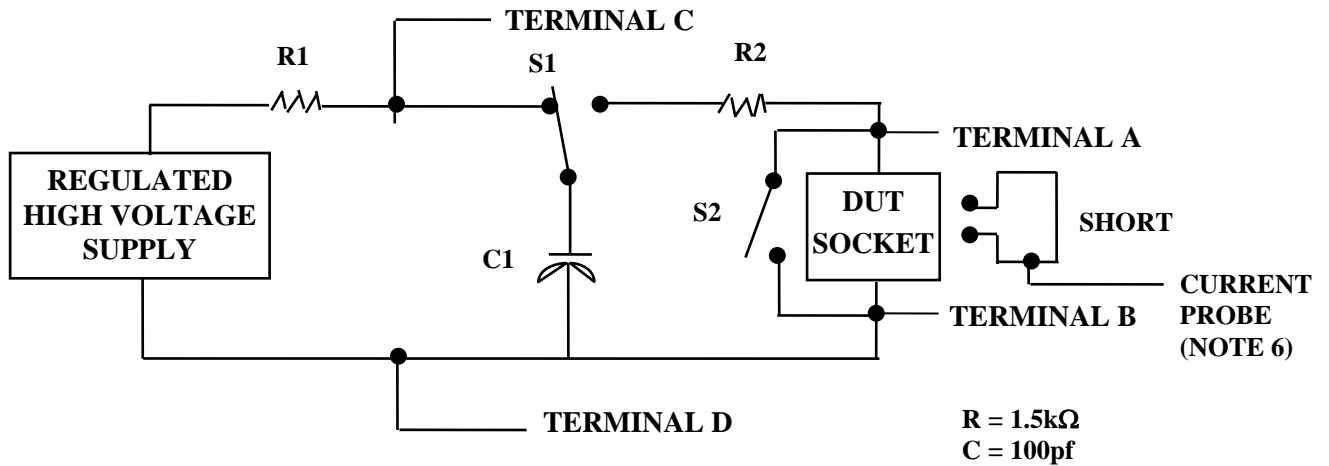
1/ Table II is restated in narrative form in 3.4 below.

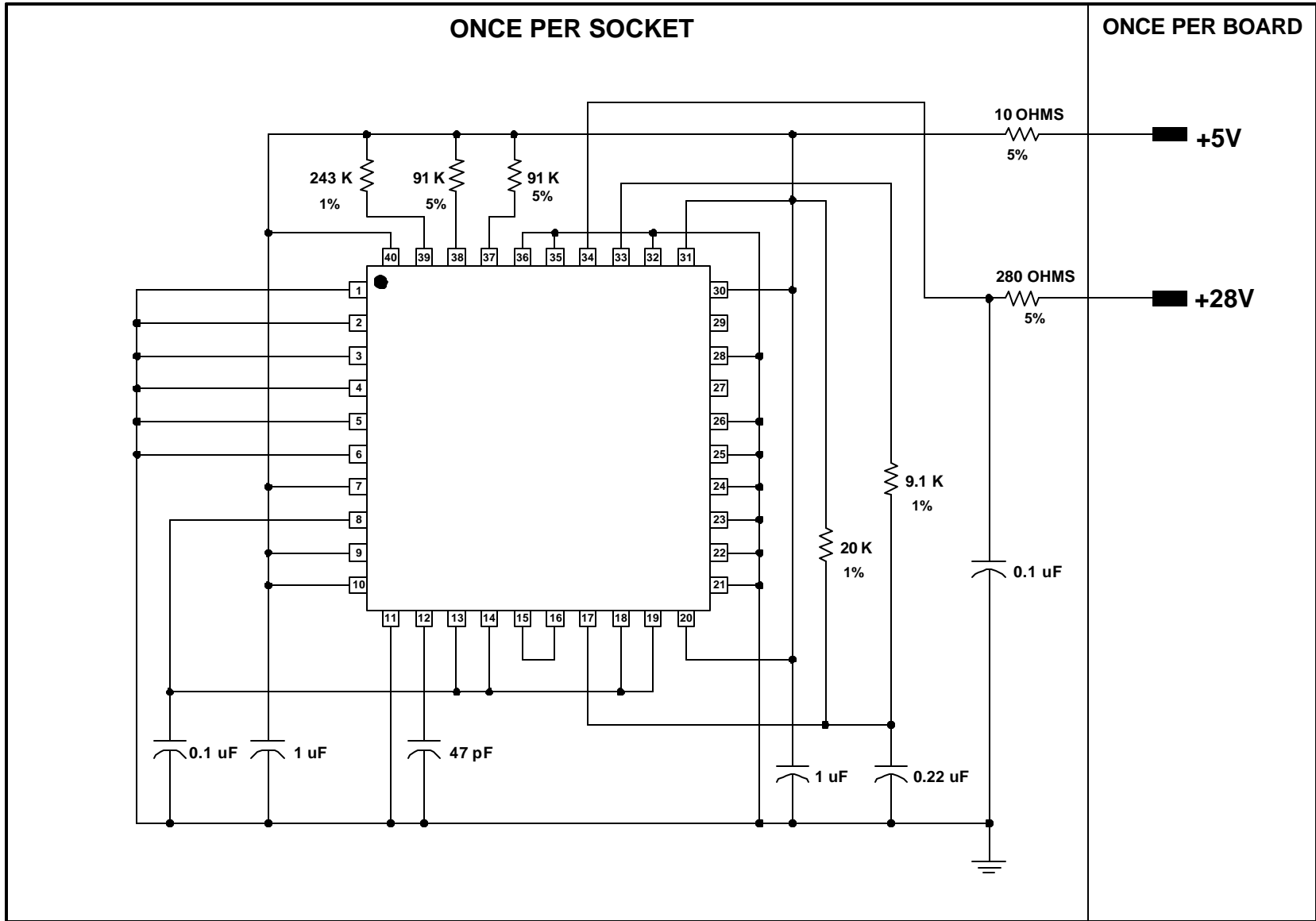
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



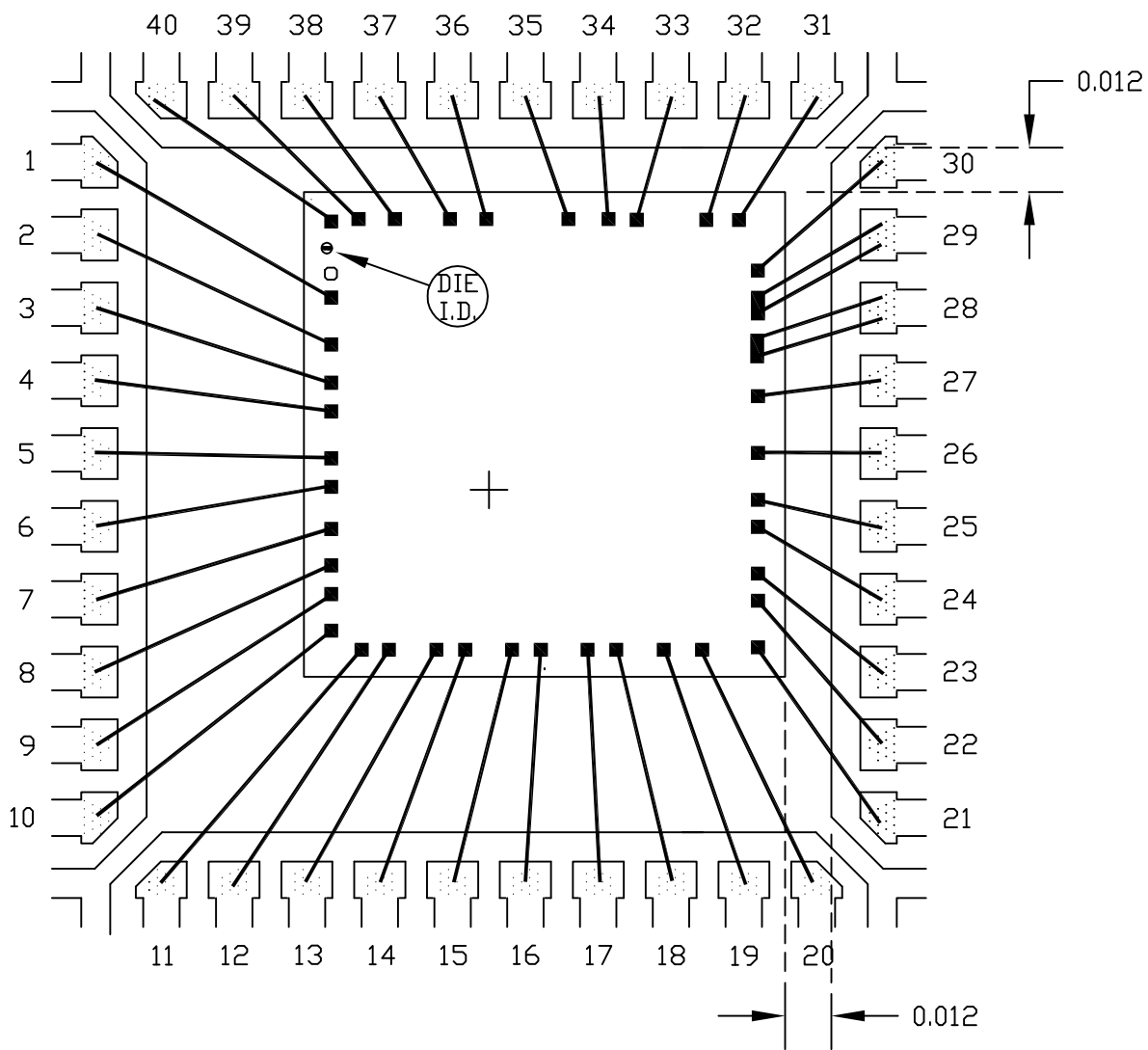


DEVICES: MAX 1907
PACKAGE: 40-QFN 6x6
MAX. EXPECTED CURRENT = 1mA (+28), 5mA (+5)

NOTES:

6x6x0.8mm THIN QFN PKG.

EXPOSED PAD PKG.



 BONDABLE AREA

PKG. CODE: T4066-5		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 185x185	PKG. DESIGN			BOND DIAGRAM #: 05-3801-0013	REV: D