RELIABILITY REPORT

FOR

MAX17480GTL+

PLASTIC ENCAPSULATED DEVICES

August 7, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX17480GTL+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX17480 is a triple-output, step-down, fixed-frequency controller for AMD's serial VID interface (SVI) CPU and northbridge (NB) core supplies. The MAX17480 consists of two high-current SMPSs for the CPU cores and one 4A internal switch SMPS for the NB core. The two CPU core SMPSs run 180° out-of-phase for true interleaved operation, minimizing input capacitance. The 4A internal switch SMPS runs at twice the switching frequency of the core SMPS, reducing the size of the external components. The MAX17480 is fully AMD SVI compliant. Output voltages are dynamically changed through a 2-wire SVI, allowing the SMPSs to be individually programmed to different voltages. A slew-rate controller allows controlled transitions between VID codes and controlled soft-start. SVI also allows each SMPS to be individually set into a low-power pulse-skipping state. Transient phase repeat improves the response of the fixed-frequency architecture, reducing the total output capacitance for the CPU core. A thermistor-based temperature sensor provides a programmable thermal-fault output (active-low VRHOT). The MAX17480 includes output overvoltage protection (OVP), undervoltage protection (UVP), and thermal protection. When any of these protection features detect a fault, the controller shuts down. True differential current sensing improves current limit and load-line accuracy. The MAX17480 has an adjustable switching frequency, allowing 100kHz to 600kHz operation per core SMPS, and twice that for the NB SMPS.

II. Manufacturing Information

A. Description/Function:	AMD 2-/3-Output Mobile Serial VID Controller
B. Process:	S4
C. Number of Device Transistors:	24311
D. Fabrication Location:	Texas
E. Assembly Location:	China, Thailand
F. Date of Initial Production:	January 24, 2009

III. Packaging Information

A. Package Type:	40-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3598
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	45°C/W
K. Single Layer Theta Jc:	1.7°C/W
L. Multi Layer Theta Ja:	28°C/W
M. Multi Layer Theta Jc:	1.7°C/W

IV. Die Information

A. Dimensions:	109 X 109 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 47 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.8 \times 10^{-9}$

$\lambda = 22.8$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S45 Process results in a FIT Rate of 0.85 @ 25C and 14.7 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The PE55 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA, 1.5x VCCMax Overvoltage per JESD78.

Table 1
Reliability Evaluation Test Results

MAX17480GTL+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	47	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data