RELIABILITY REPORT

FOR

MAX13030EEBE+
(MAX13030E-MAX13035E)

CHIP SCALE PACKAGE

April 2, 2009

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX13030EEBE+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX13030E-MAX13035E 6-channel, bidirectional level translators provide the level shifting necessary for 100Mbps data transfer in multivoltage systems. The MAX13030E-MAX13035E are ideally suited for memory-card level translation, as well as generic level translation in systems with six channels. Externally applied voltages, VCC and VL, set the logic levels on either side of the device. Logic signals present on the VL side of the device appear as a higher voltage logic signal on the VCC side of the device and vice versa. The MAX13035E features a CLK_RET output that returns the same clock signal applied to the CLK_VL input. The MAX13030E-MAX13035E operate at full speed with external drivers that source as little as 4mA output current. Each I/O channel is pulled up to VCC or VL by an internal 30Î¼A current source, allowing the MAX13030E-MAX13035E to be driven by either push-pull or open-drain drivers. The MAX13030E-MAX13034E feature an enable (EN) input that places the device into a low-power shutdown mode when driven low. The MAX13030E-MAX13035E features an automatic shutdown mode that disables the part when VCC is less than VL. The state of I/O VCC_ and I/O VL_ during shutdown is chosen by selecting the appropriate part version (see Ordering Information/Selector Guide located within the full datasheet). The MAX13030E-MAX13035E accept VCC voltages from +2.2V to +3.6V and VL voltages from +1.62V to +3.2V, making them ideal for data transfer between low-voltage ASIC/PLDs and higher voltage systems. The MAX13030E-MAX13035E are available in 16-bump UCSP (2mm x 2mm) and 16-pin TQFN (4mm x 4mm) packages, and operate over the extended -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	6-Channel High-Speed Logic-Level Translators
B. Process:	S4
C. Number of Device Transistors:	
D. Fabrication Location:	Texas
E. Assembly Location:	Texas
F. Date of Initial Production:	January 20, 2007

III. Packaging Information

A. Package Type:	16-pin UCSP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A
F. Mold Material:	N/A
G. Assembly Diagram:	#05-9000-2377
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Multi Layer Theta Ja:	121.3

IV. Die Information

A. Dimensions:	80 X 80 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 50 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 21.5 \times 10^{-9}$

$\lambda = 21.5$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S4 Process results in a FIT Rate of 4.6 @ 25C and 79.2 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The LT03 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX13030EEBE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	50	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2 & 3)				
Temperature Cycle	-40ºC/125ºC 1000 Cycles (Note 3)	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
Note 3: Ramp rate 11ºC/minute, dwell=15 minutes, One cycle/hour.