

RELIABILITY REPORT
FOR
MAX12000ETB
PLASTIC ENCAPSULATED DEVICES

August 18, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX12000 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX12000 GPS front-end amplifier IC is designed for automotive and marine GPS satellite navigation antenna modules or for any application that needs to compensate for cable losses from the GPS antenna to receiver. Two unconditionally stable low-noise amplifier stages provide the high gain and integrated I/O matching to minimize the need for external matching components and eliminate the need for additional gain stages. The MAX12000 features the option to place a bandpass ceramic or SAW filter between the two amplifier stages to provide a narrow-band output to further improve the noise performance of the GPS receiver. Additionally, a 3.4dB gain step is provided to compensate for cable loss variation between different applications.

The MAX12000 is designed to operate at the GPS frequency of 1575MHz with a 34.8dB typical cascaded gain and a 25mA supply current. The two LNA stages allow the use of a wide range of GPS filter types for maximum flexibility in system design. The final RF output pin, which drives the cable to the GPS receiver, is also the power-supply connection that accepts a DC supply in the +3.0V to +5.5V range. Alternatively, the DC supply can be applied to pin 4.

The GPS front-end amplifier is designed on a low-noise, advanced SiGe process and is available in a lead-free, 10-pin TDFN surface-mount package (3mm x 3mm).

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
RFOUT1, RFOUT2, EXTCAP to GND	-0.3V to (VCC + 0.5V)
RFIN1 Input Power (50Ω source)	+15dBm
RFIN1 to GND	-0.3V to +0.3V
RFIN2 to GND	-0.3V to +1.0V
GAIN_SELECT to GND	-0.3V to (VCC + 0.3V)
Continuous Power Dissipation (TA = +70°C)	
10-Pin TDFN (derate 18.5mW/°C above +70°C)	1481mW
Operating Ambient Temperature Range	-40°C to +105°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	1575MHz GPS Front-End Amplifier
B. Process:	GST4-MB20 Bi-CMOS Process
C. Number of Device Transistors:	555
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	April, 2006

III. Packaging Information

A. Package Type:	10-Pin Thin DFN (3x3)
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-1967
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	58 x 49 mils
B. Passivation:	Si ₃ N ₄ (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4
G. Bondpad Dimensions:	3.4 mil. Octagonal
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{1000 \times 9706 \times 76 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

△ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 1.24 \times 10^{-9} \quad \lambda = 1.24 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic #06-7242 shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-B2A**). Current monitor data for the MB20 Process results in a FIT rate of 0.22 @ 25°C and 3.83 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The WG25 die type has been found to have all pins able to withstand a transient pulse of +/-2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit).

Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX12000ETB

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 1000 hrs.	DC Parameters & functionality	76	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification packages.

Note 2: Generic package/process data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

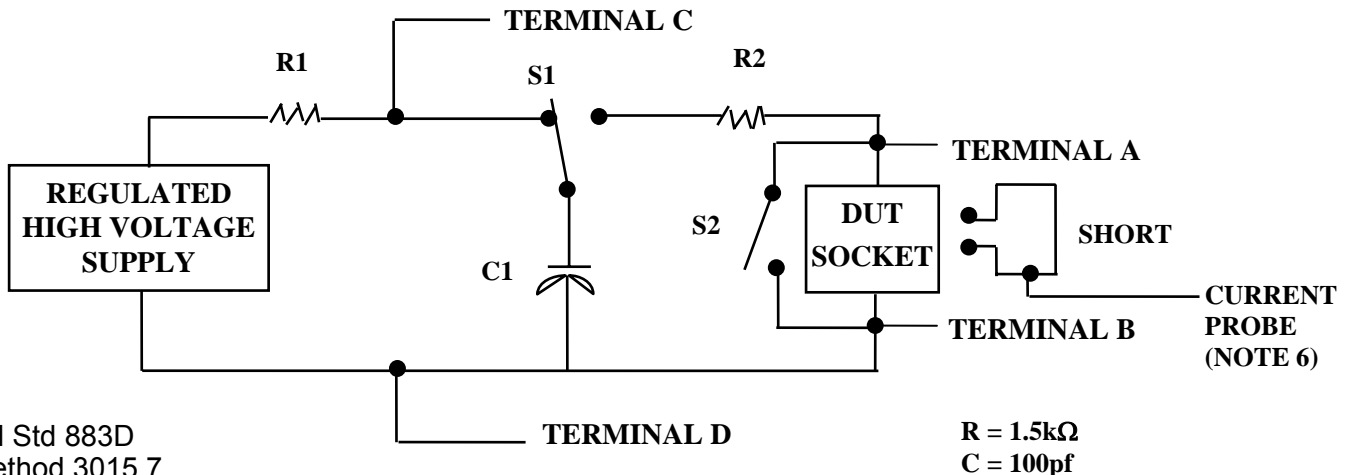
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

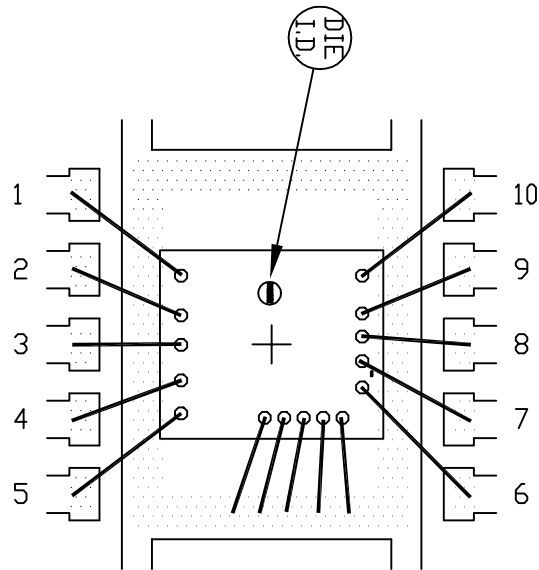
3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



3x3x0.8mm TDFN PKG.

EXPOSED PAD PKG.



 BONDABLE AREA

PKG. CODE: T1033-2		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 78x102	PKG. DESIGN			BOND DIAGRAM #: 05-9000-1967	REV: B

