

RELIABILITY REPORT  
FOR  
**MAX6315USxxDx**  
PLASTIC ENCAPSULATED DEVICES

August 7, 2001

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Reviewed by



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## Conclusion

The MAX6315 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX6315 low-power CMOS microprocessor ( $\mu$ P) supervisory circuit is designed to monitor power supplies in  $\mu$ P and digital systems. It provides excellent circuit reliability and low cost by eliminating external components and adjustments. The MAX6315 also provides a debounced manual reset input.

This device performs a single function: it asserts a reset signal whenever the  $V_{CC}$  supply voltage falls below a preset threshold or whenever manual reset is asserted. Reset remains asserted for an internally programmed interval (reset timeout period) after  $V_{CC}$  has risen above the reset threshold or manual reset is deasserted. The MAX6215's open-drain /RESET output can be pulled up to a voltage higher than  $V_{CC}$ .

The MAX6315 comes with factory-trimmed reset threshold voltages in 100mV increments from 2.5V to 5V. Preset timeout periods of 1ms, 20ms, 140ms, and 1120ms (minimum) are also available.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
$V_{CC}$	-0.3V to +6.0V
/RESET	-0.3V to +6.0V
All Other Pins	-0.3V to ( $V_{CC} + 0.3V$ )
Input Current ( $V_{CC}$ )	20mA
Output Current (/RESET)	20mA
Rate of Rise ( $V_{CC}$ )	100V/ $\mu$ s
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
4 Lead SOT-143	320mW
Derates above +70°C	
4 Lead SOT-143	4mW/°C

## II. Manufacturing Information

A. Description/Function:	Open-Drain SOT $\mu$ P Reset Circuit
B. Process:	S12 (SG1.2) - Standard 1.2 micron silicon gate CMOS
C. Number of Device Transistors:	519
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Malaysia or Thailand
F. Date of Initial Production:	June, 1996

## III. Packaging Information

A. Package Type:	<b>4 Lead SOT-143</b>
B. Lead Frame:	Alloy 42 or Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1601-0015
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

## IV. Die Information

A. Dimensions:	40 x 31 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Si
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	$\text{SiO}_2$
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 474 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

▲  
Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 2.29 \times 10^{-9} \quad \lambda = 2.29 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-4556) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The MS11-1 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2000\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 150\text{mA}$  and/or  $\pm 20\text{V}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX6315USxxDx**

<b>TEST ITEM</b>	<b>TEST CONDITION</b>	<b>FAILURE IDENTIFICATION</b>	<b>SAMPLE SIZE</b>	<b>NUMBER OF FAILURES</b>
<b>Static Life Test</b> (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	474	0
<b>Moisture Testing</b>				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	140	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
<b>Mechanical Stress</b>				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the package.

Note 2: Generic Package/Process Data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ 3/	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

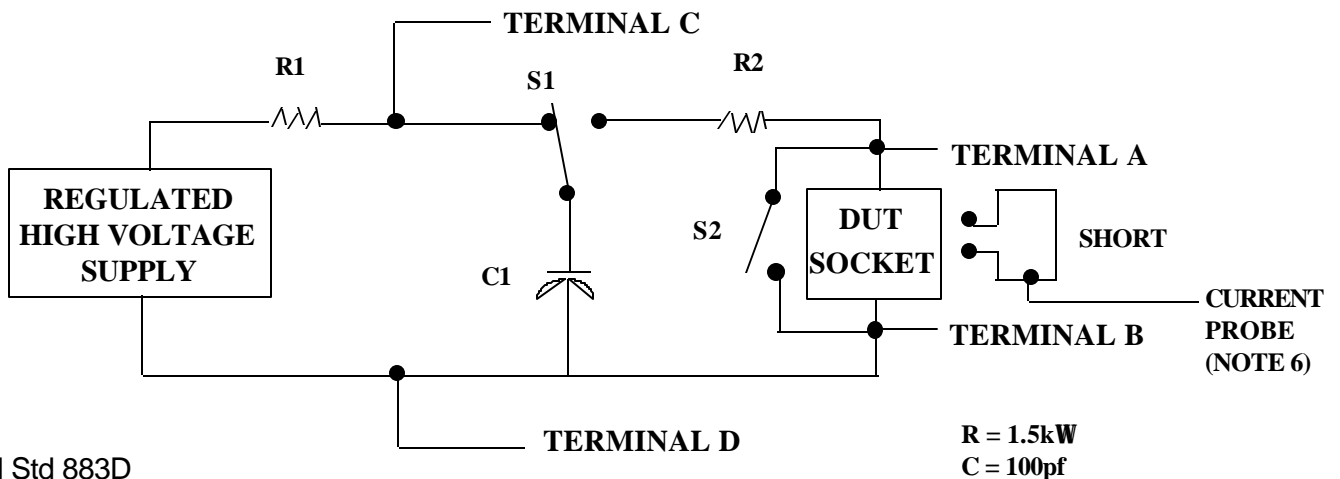
2/ No connects are not to be tested.

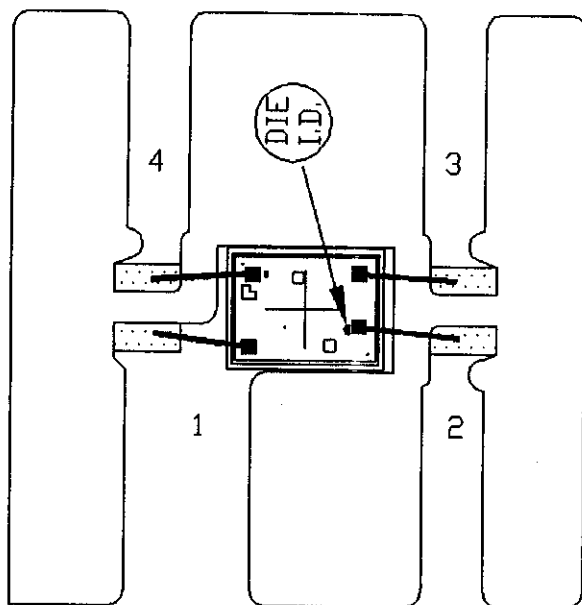
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: U4-1

CAV./PAD SIZE:  
45X32

APPROVALS

DATE

**MAXIM**

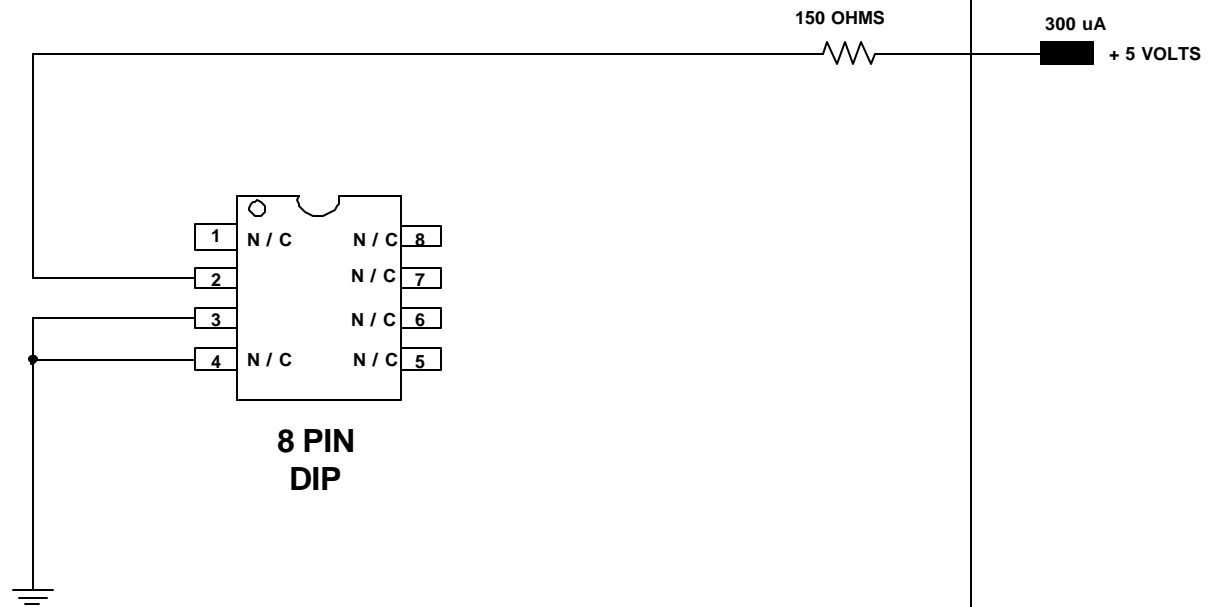
PKG.  
DESIGN

BUILDSHEET NUMBER:  
05-1601-0015

REV.:  
A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 705/706/707/708/709/809/811/812/813/821/  
822/6314/6315/6326/6327/6328  
MAX. EXPECTED CURRENT = 300 uA

NOTES: MS17 only for MAX 6326-28