

RELIABILITY REPORT
FOR
MAX4073TAxx
PLASTIC ENCAPSULATED DEVICES

April 29, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX4073T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4073T low-cost, high-side current-sense amplifier features a voltage output that eliminates the need for gain-setting resistors making it ideal for cell phones, notebook computers, PDAs, and other systems where current monitoring is crucial. High-side current monitoring does not interfere with the ground path of the battery charger making the MAX4073T particularly useful in battery-powered systems. The input common-mode range of +2V to +28V is independent of the supply voltage. The MAX4073T's wide 1.8MHz bandwidth makes it suitable for use inside battery-charger control loops.

The MAX4073T offers a high level of integration, resulting in a simple and compact current-sense solution.

The MAX4073T operates from a +3V to +28V single supply and draws only 0.5mA of supply current. This device is specified over the automotive operating temperature range (-40°C to +125°C) and is available in a space-saving 5-pin SC70 package (half the size of the SOT23).

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
VCC to GND	-0.3V to +30V
RS+, RS- to GND	-0.3V to +30V
OUT to GND	-0.3V to (VCC + 0.3V)
Output Short-Circuit to GND	Continuous
Differential Input Voltage (VRS+ - VRS-)	±5V
Current Into Any Pin	±20mA
Operating Temperature Range	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
(All voltages referenced to GND.)	
Continuous Power Dissipation (TA = +70°C)	
5-Pin SC70	200mW
6-Pin SOT23	696mW
Derates above +70°C	
5-Pin SC70	21.7mW/°C
6-Pin SOT23	8.7mW/°C

II. Manufacturing Information

A. Description/Function:	Low-Cost, SC70, Voltage-Output, High-Side Current-Sense Amplifier
B. Process:	B8
C. Number of Device Transistors:	1301
D. Fabrication Location:	California, USA
E. Assembly Location:	Philippines, Malaysia or Thailand
F. Date of Initial Production:	March, 2002

III. Packaging Information

A. Package Type:	5-Lead SC70	6-Lead SOT23
B. Lead Frame:	Copper or Alloy 42	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-2501-0159	# 05-2501-0160
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	31 x 30 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 24.13 \times 10^{-9} \quad \lambda = 24.13 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5767) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The OX69 die type has been found to have all pins able to withstand a transient pulse of 1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 50\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX4073TAxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		45	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT SC70	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

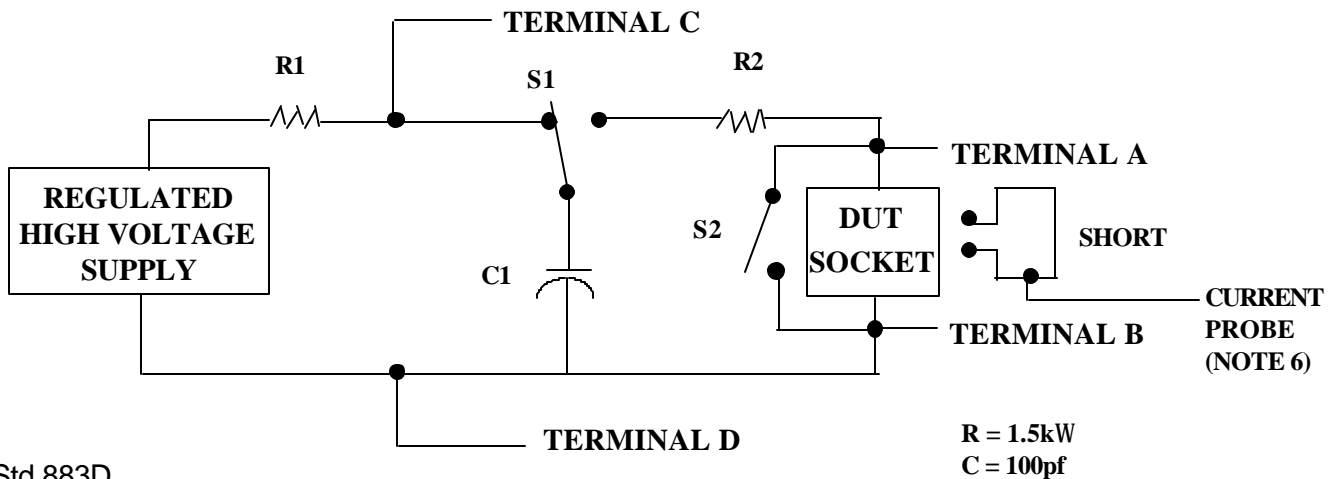
2/ No connects are not to be tested.

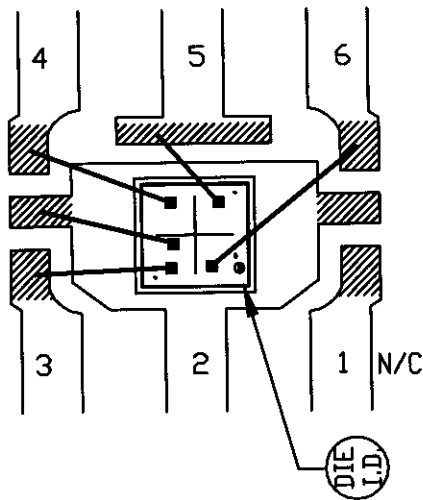
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

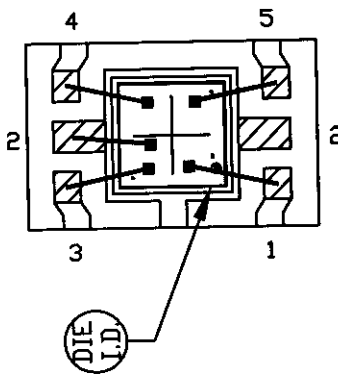
- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.






NOTE: CAVITY DOWN

PKG. CODE: U6-4		SIGNATURES /	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 64x38	PKG. DESIGN			BOND DIAGRAM #: 05-2501-0160	REV: A



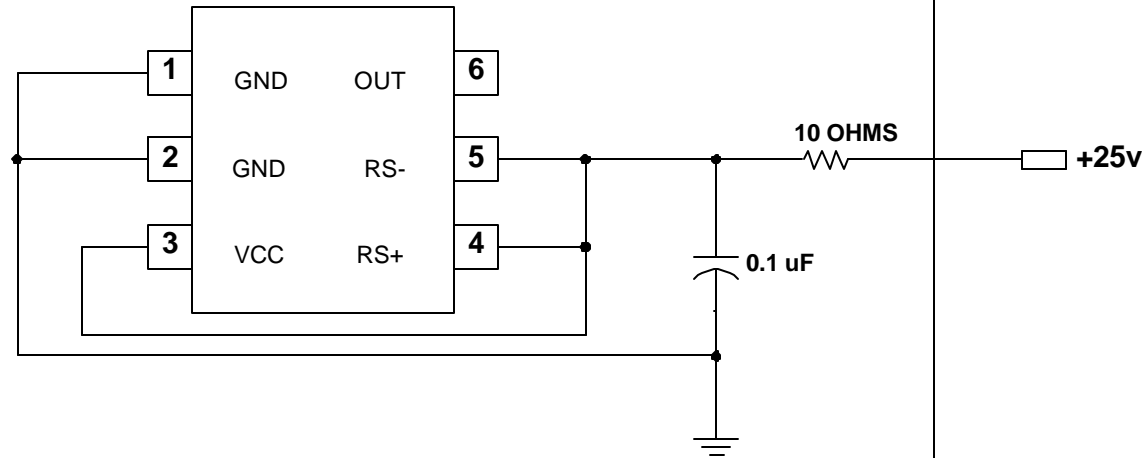
▨ BONDABLE AREA

NOTE: CAVITY DOWN

PKG. CODE: X5-1		SIGNATURES /	DATE , ,	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 35x34	PKG. DESIGN				BOND DIAGRAM #: 05-2501-0159

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 4073

DRAWN BY: HAK TAN

MAX. EXPECTED CURRENT = 2mA

NOTES: Package is 6-SOT