RELIABILITY REPORT

FOR

MAX1452xAE

PLASTIC ENCAPSULATED DEVICES

October 13, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Quality Assurance
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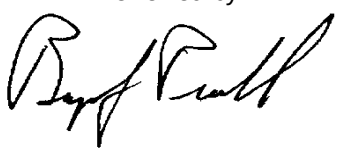
Reviewed by



Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX1452 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1452 is a highly integrated analog-sensor signal processor optimized for industrial and process control applications utilizing resistive element sensors. The MAX1452 provides amplification, calibration, and temperature compensation that enables an overall performance approaching the inherent repeatability of the sensor. The fully analog signal path introduces no quantization noise in the output signal while enabling digitally controlled trimming with the integrated 16-bit DACs. Offset and span are calibrated using 16-bit DACs, allowing sensor products to be truly interchangeable.

The MAX1452 architecture includes a programmable sensor excitation, a 16-step programmable-gain amplifier (PGA), a 768-byte (6144 bits) internal EEPROM, four 16-bit DACs, an uncommitted op amp, and an on-chip temperature sensor. In addition to offset and span compensation. The MAX1452 provides a unique temperature compensation strategy for offset TC and FSOTC that was developed to provide a remarkable degree of flexibility while minimizing testing costs.

The MAX1452 is packaged for the commercial, industrial, and automotive temperature ranges in 16-pin SSOP packages.

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage, VDD to VSS	-0.3V, +6V
All Other Pins	(VSS - 0.3V) to (VDD + 0.3V)
Short-Circuit Duration, FSOTC, OUT, BDR, AMPOUT	Continuous
Operating Temperature:	
MAX1452CAE	0°C to +70°C
MAX1452EAE	-40°C to +85°C
MAX1452AAE	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Continuous Power Dissipation (TA = +70°C)	
16-Lead SSOP	640mW
Derates above +70°C	
16-Lead SSOP	8.00mW/°C

II. Manufacturing Information

A. Description/Function:	Low-Cost Precision Sensor Signal Conditioner
B. Process:	TC05
C. Number of Device Transistors:	67,382
D. Fabrication Location:	Taiwan, USA
E. Assembly Location:	Malaysia or Phillipines
F. Date of Initial Production:	April, 2000

III. Packaging Information

A. Package Type:	**10-Lead uMAX**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-2701-0003
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	91 x 82 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/Si/Cu (Aluminum/ Silicon/ Copper)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal 1: 0.9 microns; Metal 2: 0.9 microns (as drawn)
F. Minimum Metal Spacing:	Metal 1: 0.8 microns; Metal 2: 0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 126 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 8.62 \times 10^{-9}$ $\lambda = 8.62$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. The Burn-In Schematic #06-5698 shows the static circuit used for this test Maxim performs failure analysis on lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The SC02 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±50mA.

Table 1
Reliability Evaluation Test Results

MAX1452xAE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	126	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic Package/Process Data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

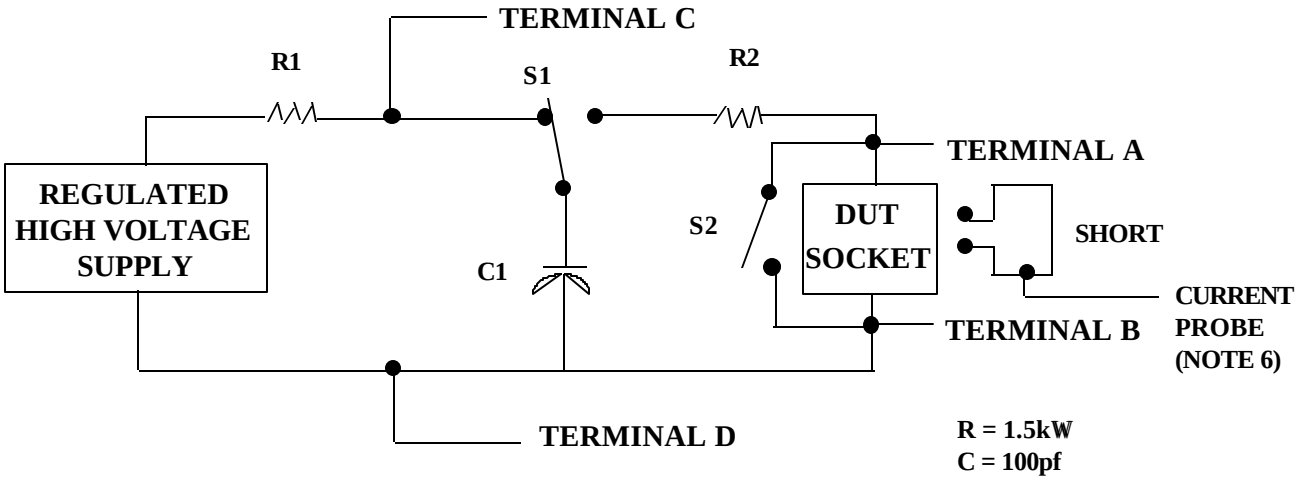
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

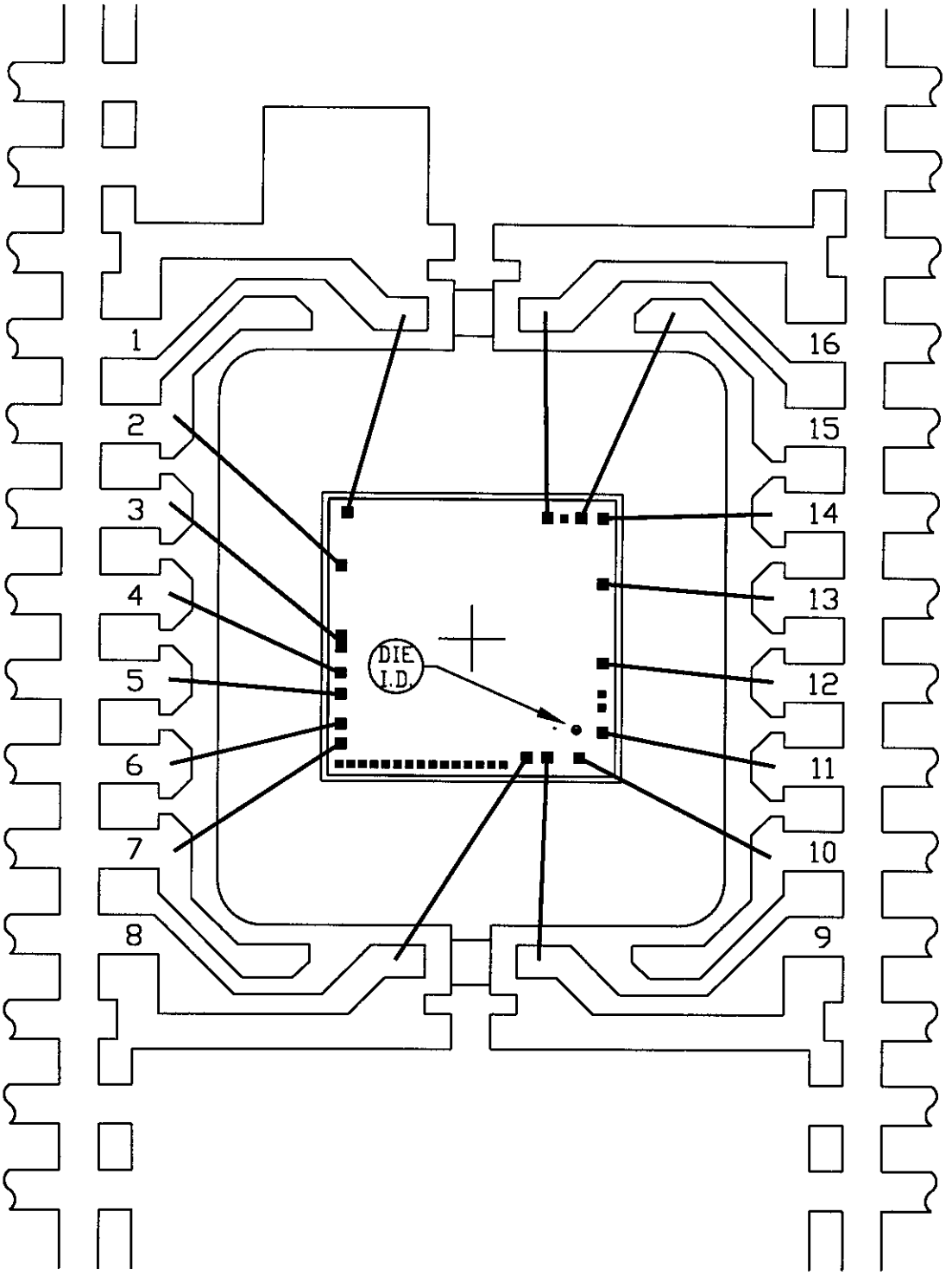
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

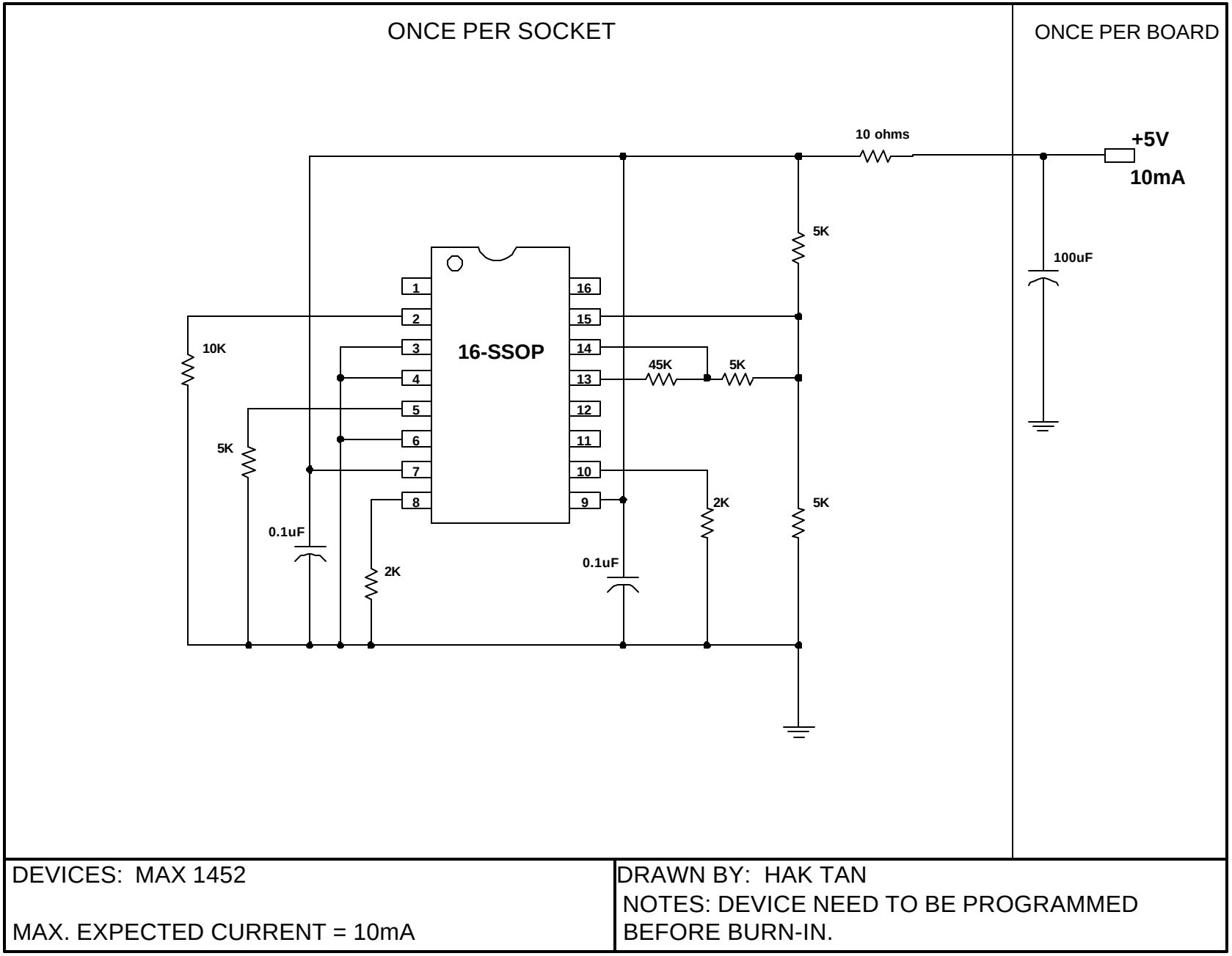
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE: A16-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 154X173	PKG. DESIGN			BOND DIAGRAM #: 05-2701-0003	REV: A



DEVICES: MAX 1452

MAX. EXPECTED CURRENT = 10mA

DRAWN BY: HAK TAN

NOTES: DEVICE NEED TO BE PROGRAMMED BEFORE BURN-IN.