RELIABILITY REPORT

FOR

**MAX1239EEE**

PLASTIC ENCAPSULATED DEVICES

January 23, 2003

# MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

Bryan J. Preeshl
Quality Assurance
Executive Director

## Conclusion

The MAX1239 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents



## I. Device Description

A. General

The MAX1239 low-power, 12-bit, multichannel analog-to-digital converter (ADCs) features internal track/hold (T/H), voltage reference, clock, and an I 2 C™-compatible 2-wire serial interface. This device operates from a single supply of 2.7V to 3.6V and require only 670µA at the maximum sampling rate of 94.4ksps. Supply current falls below 230µA for sampling rates under 46ksps. AutoShutdown™ powers down the device between conversions, reducing supply current to less than 1µA at low throughput rates. The MAX1239 has 12 analog input channels each. The fully differential analog inputs are software configurable for unipolar or bipolar, and single ended or differential operation. The full-scale analog input range is determined by the internal reference or by an externally applied reference voltage ranging from 1V to VDD. The MAX1239 features a 2.048V internal reference and is available in a 16-pin QSOP package. The MAX1239 is guaranteed over the extended temperature range (-40°C to +85°C). For pin-compatible 10-bit parts, refer to the MAX1136–MAX1139 data sheet. For pin-compatible 8-bit parts, refer to the MAX1036–MAX1039 data sheet.

B. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| $V_{DD}$ to GND | -0.3V to +6V |
| AIN0–AIN11, REF to GND | -0.3V to the lower of ($V_{DD}$ + 0.3V) and 6V |
| SDA, SCL to GND | -0.3V to +6V |
| Maximum Current Into Any Pin | ±50mA |
| Continuous Power Dissipation (TA = +70°C) | |
| 16-Pin QSOP | 666.7mW |
| Derates above +70°C | |
| 16-Pin QSOP | 8.3mW/°C |
| Operating Temperature Range | -40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -60°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | 2.7V to 3.6V Low-Power, 4-/12-Channel, 2-Wire Serial, 12-Bit ADCs |
| B. Process: | S6 (Standard 0.6 micron silicon gate CMOS) |
| C. Number of Device Transistors: | 12,956 |
| D. Fabrication Location: | California, USA |
| E. Assembly Location: | Philippines, Korea or Thailand |
| F. Date of Initial Production: | January, 2002 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | **16-Pin QSOP** |
| B. Lead Frame: | Copper |
| C. Lead Finish: | Solder Plate |
| D. Die Attach: | Silver-filled Epoxy |
| E. Bondwire: | Gold (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #05-2101-0044 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: | Level 1 |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 86 x 80 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Aluminum/Si (Si = 1%) |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 0.6 microns (as drawn) |
| F. Minimum Metal Spacing: | 0.6 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-9}$

$\lambda$ = 13.57 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5748) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AC31-1 die type has been found to have all pins able to withstand a transient pulse of ±2500V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±100mA and/or ±20V.

**Table 1**
Reliability Evaluation Test Results

**MAX1239EEE**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | | 80 | 0 |
| **Moisture Testing** (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | QSOP | 77 | 0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters<br>& functionality | | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters | | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

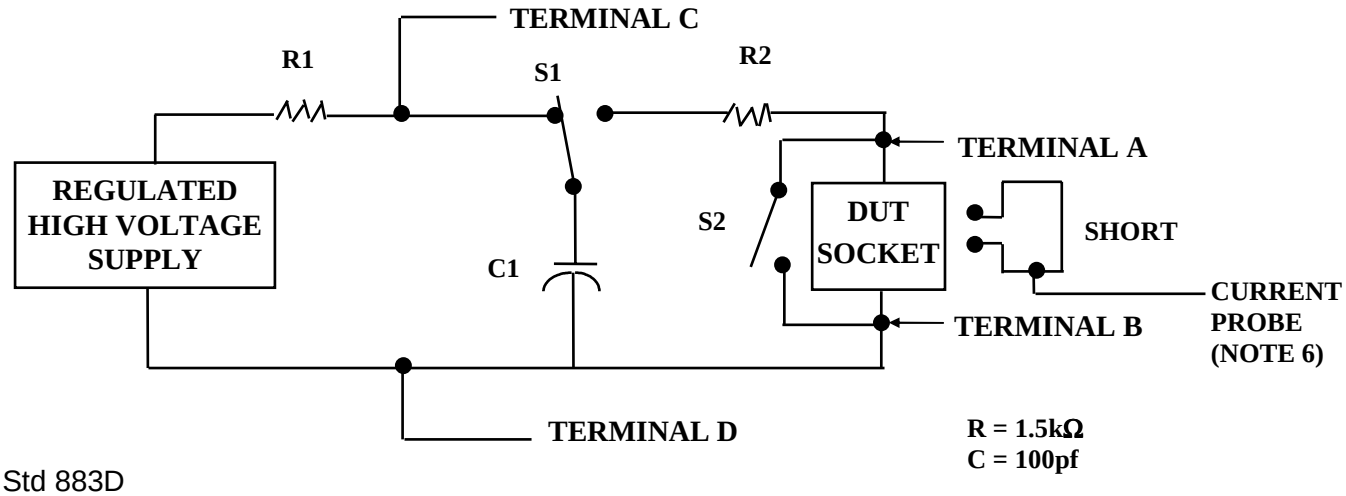
(e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

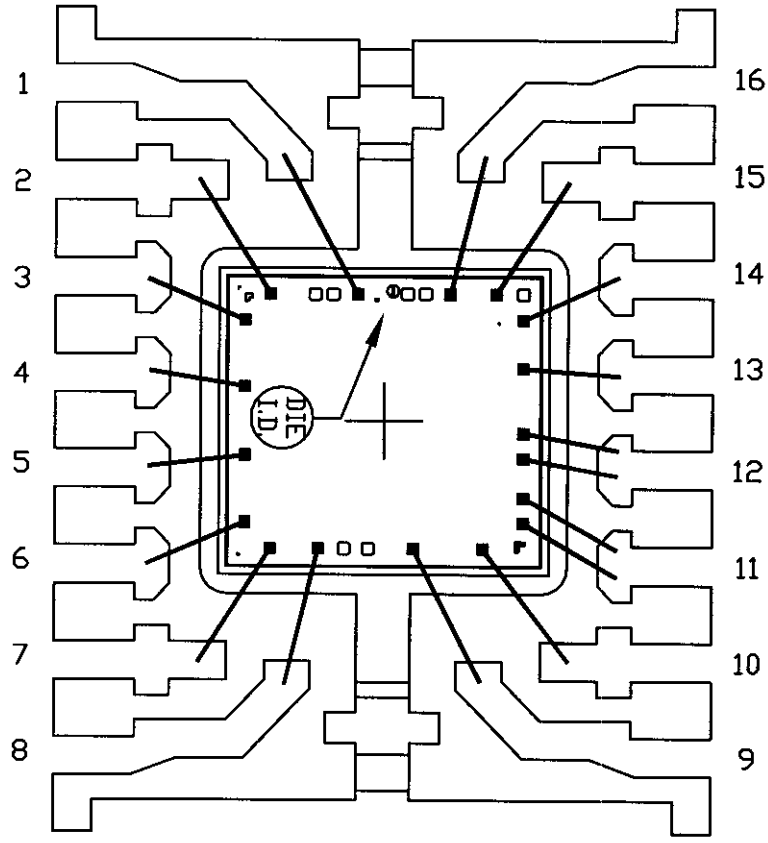
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

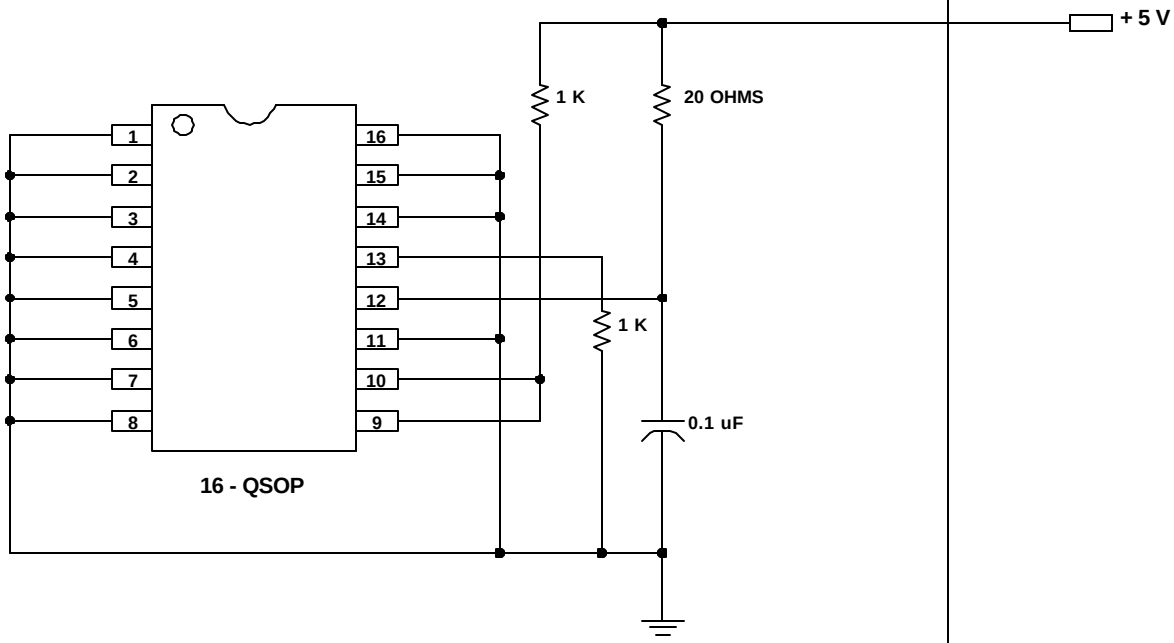





| | | | | |
|---|---|---|---|---|
| PKG. CODE: E16-4 | | SIGNATURES | DATE | MAXIM CONFIDENTIAL & PROPRIETARY |
| CAV./PAD SIZE: 96X90 | PKG. DESIGN | | | BOND DIAGRAM #: 05-2101-0044 REV: A |

ONCE PER SOCKET

**ONCE PER BOARD**




DEVICES: MAX 1138/9 AND MAX 1238/9

MAX. EXPECTED CURRENT = 500uA

DRAWN BY: HAK TAN

NOTES: