

RELIABILITY REPORT
FOR
MAX1039AEEE
PLASTIC ENCAPSULATED DEVICES

September 2, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX1039 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1039 low-power, 8-bit, multichannel, analog-to-digital converter (ADC) features internal track/hold (T/H), voltage reference, clock, and an I²C-compatible 2-wire serial interface. This device operates from a single supply and requires only 350 μ A at the maximum sampling rate of 188ksps. AutoShutdown™ powers down the devices between conversions reducing supply current to less than 1 μ A at low throughput rates. The MAX1039 has twelve analog input channels. The analog inputs are software configurable for unipolar or bipolar and single-ended or pseudo-differential operation.

The full-scale analog input range is determined by the internal reference or by an externally applied reference voltage ranging from 1V to V_{DD}. The MAX1039 features a 2.048V internal reference.

The MAX1039 is available in a 16-pin QSOP packages. The MAX1039 is guaranteed over the extended industrial temperature range (-40°C to +85°C).

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
VDD to GND	-0.3V to +6V
AIN0–AIN11, REF to GND	-0.3V to the lower of (VDD + 0.3V) and +6V
SDA, SCL to GND	-0.3V to +6V
Maximum Current Into Any Pin	±50mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin QSOP	667mW
Derates above +70°C	
16-Pin QSOP	8.3mW/°C

II. Manufacturing Information

- A. Description/Function: 2.7V to 5.5V, 12-Channel 2-Wire Serial 8-Bit ADCs
- B. Process: S6 BiCMOS process
- C. Number of Device Transistors: 7257
- D. Fabrication Location: California, USA
- E. Assembly Location: Korea, Thailand or Philippines
- F. Date of Initial Production: March, 2002

III. Packaging Information

- A. Package Type: **16-Lead QSOP**
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate
- D. Die Attach: Conductive Epoxy
- E. Bondwire: Gold (1 mil dia.)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: Buildsheet # 05-2101-0050
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

- A. Dimensions: 67 x 63 mils
- B. Passivation: $\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
- C. Interconnect: TiW/ AlCu/ TiWN
- D. Backside Metallization: None
- E. Minimum Metal Width: .6 microns (as drawn)
- F. Minimum Metal Spacing: .6 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric: SiO_2
- I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 158 \times 2} \text{ (Chi square value for MTTF upper limit)}$$

△ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 6.87 \times 10^{-9} \quad \lambda = 6.87 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-5778) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**) located on the Maxim website at <http://www.maxim-ic.com>.

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AC33-1 die type has been found to have all pins able to withstand a transient pulse of $\pm 2500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX1039AEEE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	158	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

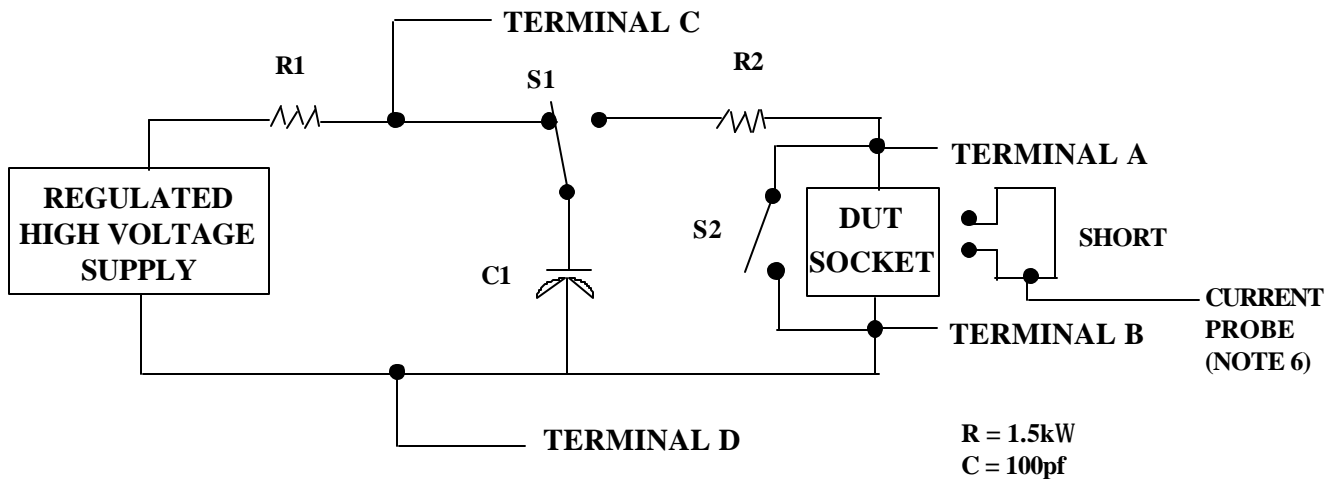
2/ No connects are not to be tested.

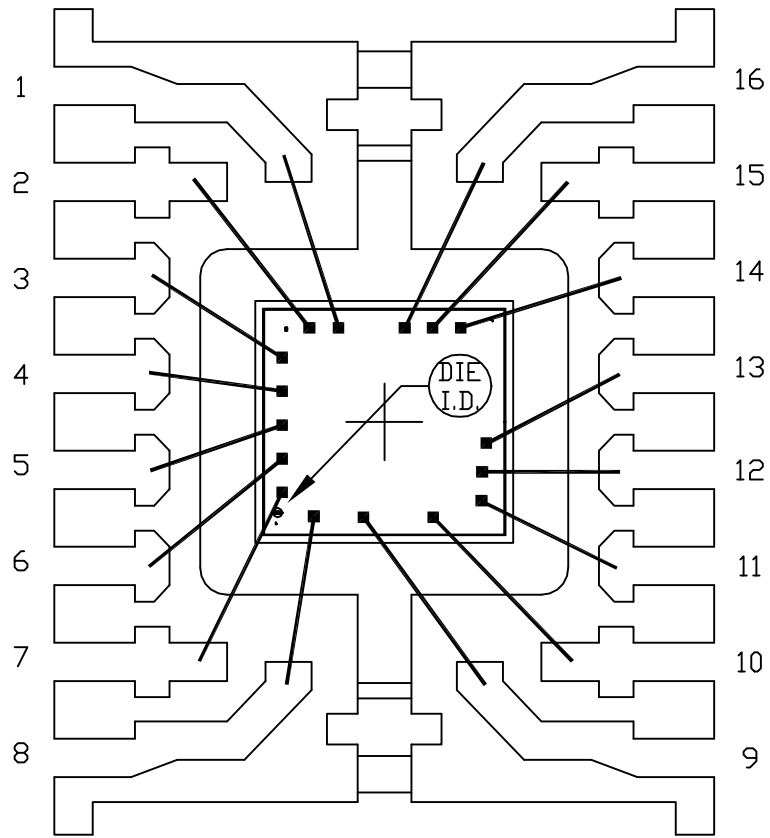
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND , $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

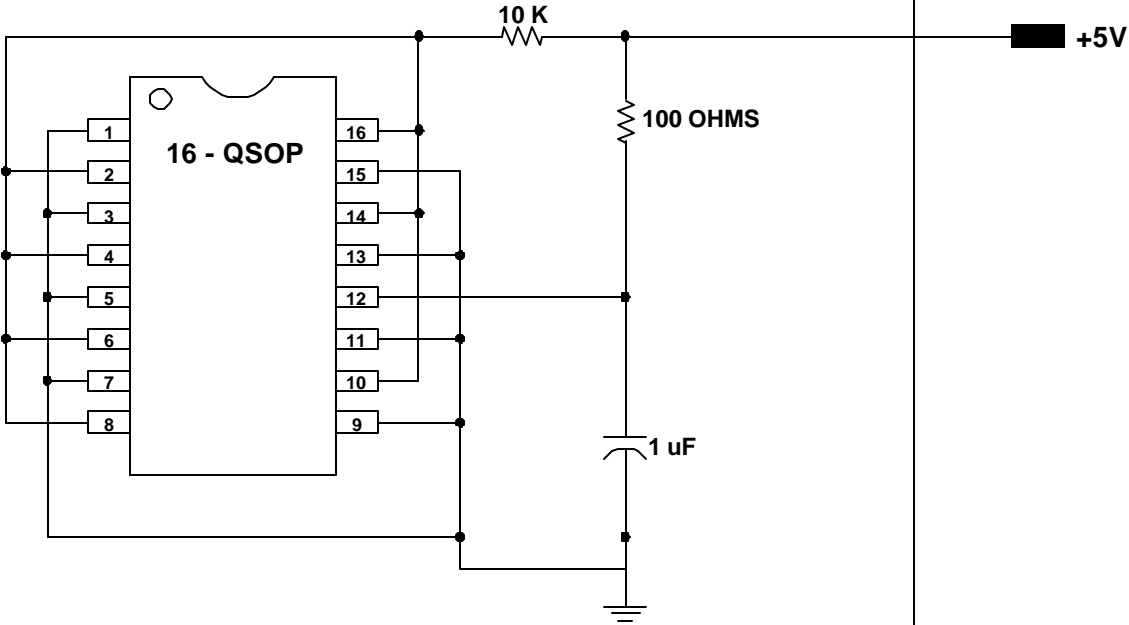




PKG. CODE: E16-4		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 96X90	PKG. DESIGN		3/2/01	BOND DIAGRAM #:	REV:
			3/5/01	05-2101-0050	A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 1038/1039

DRAWN BY: HAK TAN

MAX. EXPECTED CURRENT =10 uA

NOTES: