December 1997

RR-B2A

High-Frequency Bipolar Products Reliability Report

This report presents the product reliability data for Maxim's High-Frequency Bipolar analog and digital products. This data was collected from extensive reliability stress tests performed between June 1, 1994 and January 1, 1997. It is separated into five major fabrication processes: 1) SHPi, 9.3GHz two-layer bipolar, 2) GST-1, 12GHz three-layer bipolar, 3) GST-2, 27GHz three-layer bipolar, 4) CPi, 9.3GHz two-layer with complementary vertical PNP devices to 5.5GHz, and 5) CB2, 9.4GHz two-layer with complementary vertical PNP devices to 8.7GHz.

During this testing period, over 3.4 million device operating hours were accumulated for products at an operating junction temperature of +150°C to +165°C. The data in this report is typical of Maxim's production products. As you will see, Maxim's high-frequency bipolar products demonstrate the same high level of reliability you have become accustomed to with our other products and processes.

High-Frequency Bipolar Products Reliability Report

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Fabrication Processes

Maxim is currently running five major high-frequency bipolar processes:

SHPi (f_T = 9.3GHz, two layer)
GST-1 (f_T = 12GHz, three layer)
GST-2 (f_T = 27GHz, three layer)
CPi (f_T = 9.3GHz NPN, 5.5GHz PNP)
CB2 (f_T = 9.4GHz NPN, 8.7GHz PNP)

SHPi

SHPi is a recessed-oxide-isolated, high-speed, NPN bipolar process designed for superior performance and flexibility. It features high-performance vertical NPN transistors (f_T = 9.3GHz at V_{CE} = 4V, f_{MAX} = 12GHz at V_{CE} = 4V). Minimum NPN transistor area is 8µm x 20µm. The process features two layers of gold interconnect on 4µm pitch.

GST-1

GST-1 (Giga-Speed Si-Bipolar Technology) is a high-speed, self-aligned double-polysilicon process. GST-1 was designed for building high-density, high-performance circuits with up to three layers of gold interconnect. The process employs many techniques, such as Reactive Ion Etching (RIE) and trench isolation, to provide a silicon bipolar platform for high-performance circuit applications to 12GHz.

GST-2

Like GST-1, GST-2 is a high-speed, self-aligned double-polysilicon process. The platform was designed for building high-density, high-performance circuits, and employs many of the same processing features as GST-1. GST-2, however, achieves GaAs speed to 27GHz without GaAs pricing, for up to 200,000 transistors per die.

CPi

Like SHPi, CPi is a recessed-oxide-isolated, high-speed, complementary bipolar process designed for superior performance and flexibility. Unique to CPi is an optional dual-gate P-channel JFET with one extra mask. However, the feature which most differentiates this process from SHPi is the availability of complementary vertical PNP transistors with f_T = 5.5GHz at V_{CE} = 4V.

CB2

CB2 is a single poly-emitter, recessed-oxide-isolated, high-speed complementary bipolar process. It is optimized for low-voltage applications and applications from 12V to 20V. Like CPi, this process offers the availability of vertical PNP transistors with f_{MAX} of approximately 8.7GHz, to complement NPN transistors with f_{MAX} of approximately 9.4GHz at V_{CE} = 4V.

Reliability Methodology

Maxim's approach to reliability testing is conservative. Each of the high-frequency bipolar processes is qualified using industry-standard tests and methods as shown in Table 1.

See *Infant Mortality Evaluation* section for infant mortality data and evaluations on high-frequency bipolar processes in our Beaverton fabrication facility. Each failure category is prioritized by its relative frequency, to identify which failure mode should be addressed first, second, and so on. This data demonstrates Maxim's goal to provide our customers with the lowest overall cost solution through superior quality products.

Maxim's SHPi, GST-1, GST-2, CPi, and CB2 high-frequency bipolar processes clearly meet or exceed the performance and reliability expectations of the semiconductor industry. Cross-sectional views of these five processes are shown in Figures 1–4.

TABLE 1: MAXIM PROCESS RELIABILITY TESTS

TEST NAME	CONDITIONS	SAMPLING PLAN (ACC/SS)
Life Test	+150°C (T_j)/1000 hrs	1/77 or 0/45 (LTPD = 5)
85/85	+85°C, 85% RH, 1000 hrs cycled bias	1/77 or 0/45 (LTPD = 5)
Pressure Pot	+121°C, 100% RH, 15 PSIG, 168 hrs, unbiased	1/77 or 0/45 (LTPD = 5)
Temperature Cycling	-55°C to +125°C, air to air, 1000 cycles	1/77 or 0/45 (LTPD = 5)
High-Temperature Storage	+150°C, 1000 hrs, unbiased	1/77 or 0/45 (LTPD = 5)

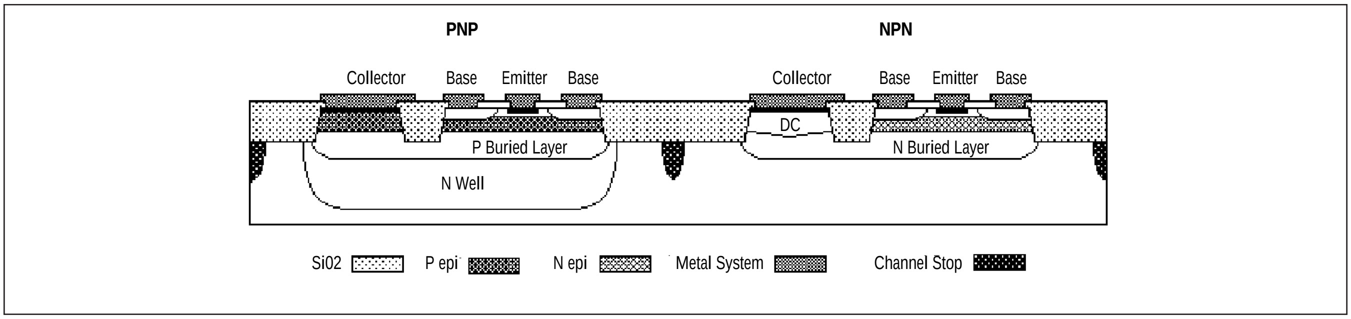

Figure 1: SHPI (NPN Transistor) and CPI (NPN and PNP Transistor) Process

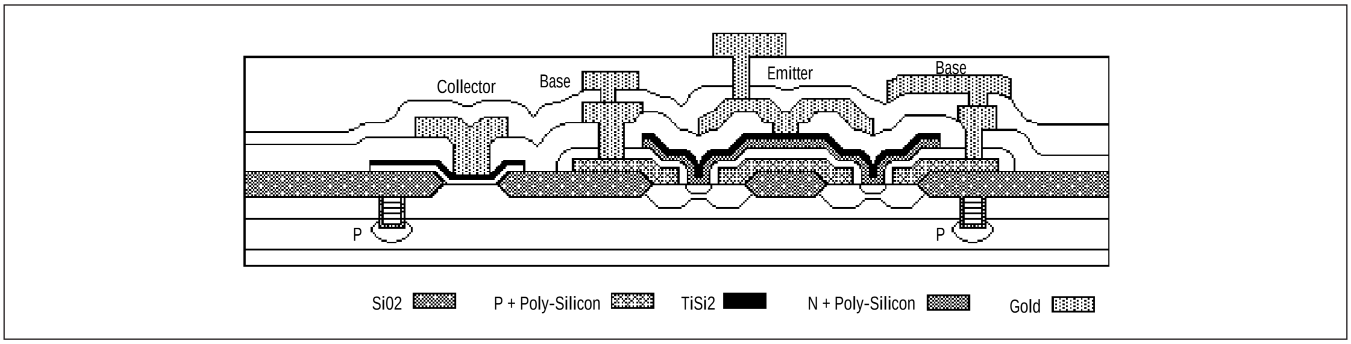

Figure 2: GST-1 Process (NPN Transistor)

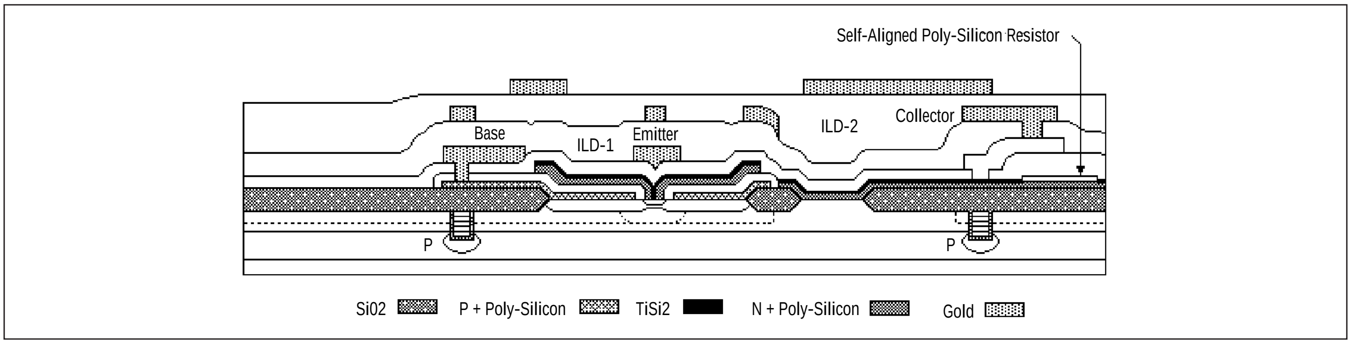

Figure 3: GST-2 Process (NPN Transistor)

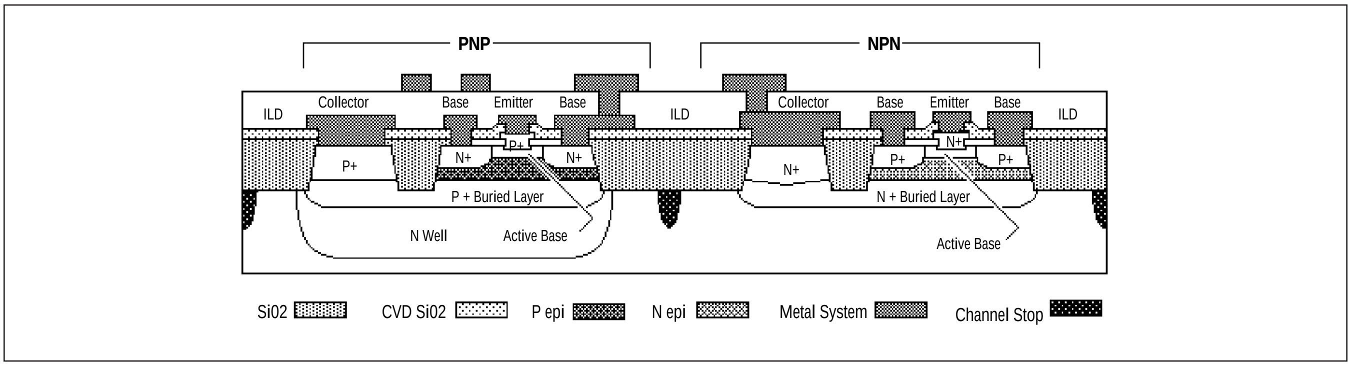

Figure 4: CB2 Process (PNP Transistor and NPN Transistor)

High-Frequency Bipolar Products Reliability Report

Reliability Strategy

Reliability Program

Maxim has implemented a series of Quality and Reliability programs aimed at building the highest quality, most reliable analog products in the industry. All products, processes, packages, and changes in manufacturing steps must be subjected to Maxim's reliability testing before release to manufacturing for mass production. Our reliability program includes:

Step 1: Initial Reliability Qualification Program
Step 2: Ongoing Reliability Monitor Program
Step 3: In-Depth Failure Analysis and Corrective Action

Tables 4–8 show the results of long-term life testing for each process. Tables 9–12 show similar information for 85/85, Pressure Pot, Temperature Cycling, and High-Temperature Storage testing.

Step 1: Initial Reliability Qualification Program

Maxim's product reliability test program meets EIA-JEDEC standards, and most standard OEM reliability test requirements.

Table 1 summarizes the qualification tests that comprise part of Maxim's reliability program. We require that three consecutive manufacturing lots from a new process technology successfully meet these reliability test requirements before releasing products.

Step 2: Ongoing Reliability Monitor Program

Maxim identifies specific products from each of the high-frequency bipolar processes on which to perform reliability monitor testing. Each part is subjected to 1000 hours of High-Temperature Operating Life testing, and 168 hours of Pressure Pot testing.

Step 3: Failure Analysis and Corrective Action

With our technical failure analysis staff, we are capable of handling in-depth analysis of every reliability test failure to the device level. If an alarming reliability failure mechanism or trend is identified, the corrective action will be initiated automatically. This proactive response and feedback ensures that any device failure mechanism will be corrected before it becomes a major problem.

Designed-In High Reliability

A disciplined design methodology is an essential ingredient in the manufacturing of a reliable part. No amount of finished product testing can create reliability in a marginal design.

To design-in reliability, Maxim has formulated a set of physical layout rules that yield reliable products, even under worst-case manufacturing tolerances. These rules are rigorously enforced, and every circuit is subjected to computerized Design Rule Checks to ensure compliance.

Maxim pays special attention to Electrostatic Discharge (ESD) protection. Our goal is to design every pin of every product to withstand ESD voltages in excess of 2000 Volts, with the use of a number of available protection schemes. In some cases, implementing protection schemes can limit frequency response, which is unacceptable. In those instances, we take special care to fully identify the ESD hazard level, following the guidelines defined in MIL-STD-883, method 3015. Of course, we use ESD shielding materials to make sure all products are afforded high levels of ESD protection in storage and transit.

Wafer Inspection

All wafers are fabricated using stable, proven processes with extremely tight control. Each wafer must pass numerous in-process check points, such as oxide thickness, alignment, critical dimensions, defect densities, etc., and must comply with Maxim's demanding electrical and physical specifications.

Finished wafers are inspected optically to detect any physical defects (this is similar to the visual inspection requirements of MIL-STD-883, method 2010).

Reliability Testing

Life Test

Life testing is performed using static bias conditions that simulate long-term use under application conditions. This test estimates the product's field performance over a long time frame. It establishes, through calculations based on Life Test results, the constant failure-rate level (in FITs), and helps identify any early wearout mechanisms. The device under test is operated at a controlled, elevated ambient temperature to ensure device junctions are at +150°C. This test can be used to detect design, manufacturing, silicon contamination, metal integrity, and assembly-related defects.

Table 2 summarizes the data from Life Tests conducted at Maxim's high-frequency bipolar fabrication facility in Beaverton, Oregon. Tables 4–8 display Life Test data for several individual products manufactured on each of those processes.

For information on calculating the failure rates of these products and processes, refer to Appendix 1 of this report.

Test: High-Temperature Operating Life (Life Test)
Test Conditions: +150°C operating junction temperature, static bias, 100% duty cycle
Failure Criteria: Must meet data sheet specifications
Results: See Table 2 and Tables 4–8

85/85 (Temperature/Humidity Bias) Test

The most popular integrated circuit (IC) packaging material is plastic. Plastic packages are not hermetic, therefore moisture and other contaminants can enter the package. Humidity testing can help determine the effects of those contaminants, and may help establish the long-term effects of operating under high levels of humidity.

Maxim tests plastic encapsulated or other non-hermetic packaged products for resistance to long-term effects of moisture using the 85/85 or Temperature/Humidity Bias (THB) test. In addition to 85/85 testing, Pressure Pot and HAST (Highly Accelerated Stress Test) can also be used as evaluation tools.

In the 85/85 test, the device is placed in an atmosphere of +85°C temperature and 85% relative humidity for a period of at least 1000 hours, with bias applied. Most of the high-performance bipolar products tested in our Beaverton facility dissipate enough power so that, if operated with continuous bias, moisture would not penetrate the package. Therefore, we operate the parts at 20% duty cycle (for example, 5 minutes on, 25 minutes off) to ensure that moisture enters the package.

Test: Temperature/Humidity Bias (85/85)
Test Conditions: +85°C ambient temperature, 85% relative humidity, static cycled bias (20% duty cycle)
Failure Criteria: Must meet data sheet specifications
Results: See Table 9

Pressure Pot Test

The Pressure Pot test simulates a product's exposure to atmospheric humidity. The object of this evaluation is to cause any corrosive contaminants to react at the die level or bond pads.

Test: Pressure Pot
Test Conditions: +121°C ambient temperature, 100% relative humidity, 15 PSIG pressure, unbiased, 168 hours
Failure Criteria: Must meet data sheet specifications
Results: See Table 10

TABLE 2: LIFE TEST DATA SUMMARY

PROCESS FAMILY	NUMBER OF LOTS TESTED	NUMBER OF FAILURES	TOTAL UNITS TESTED	DEGREES OF FREEDOM	FAILURES IN TIME (FITs)			
					+25°C REF		+75°C REF	
					60%	90%	60%	90%
SHPi	35	0	1507	2	0.06	0.15	5.40	13.50
GST-1	45	0	1720	2	0.08	0.20	7.14	18.00
GST-2	9	0	464	2	0.20	0.51	17.90	45.00
CPi	4	0	183	2	0.40	1.01	35.40	89.10
CB2	3	0	75	2	1.20	3.09	108.00	272.00

HAST Test

HAST (Highly Accelerated Steam and Temperature, sometimes referred to as Highly Accelerated Stress Test) is replacing 85/85 testing in many instances. Experiments conducted throughout the industry have shown that the effects of HAST closely duplicate the effects of 85/85 testing, but in one-tenth the time. Thus, a 1000 hour 85/85 test could be completed in 100 hours through HAST testing. This is an extremely useful test to use for corrective-action verification and/or design-change verification.

Test:	HAST
Test Conditions:	+120°C ambient temperature, 85% relative humidity, 9 PSIG pressure, biased, 100 hours minimum
Failure Criteria:	Must meet data sheet specifications

Temperature-Cycling Test

The Temperature-Cycling test measures a component's response to temperature changes and construction quality. The test cycles parts through a predetermined temperature range (MIL-STD-883, method 1010, class B: -55°C to +125°C, class C: -65°C to +150°C). Fabrication and assembly problems can both be discovered using this test, but it typically identifies any potential quality problems.

Test:	Temperature Cycling
Test Conditions:	-55°C air, +125°C air, transition time less than 60 seconds, 15 minute dwell, 1000 cycles
Failure Criteria:	Must meet data sheet specifications
Results:	See Table 11

High-Temperature Storage Test

The High-Temperature Storage test evaluates changes in a product's performance following long-term storage at elevated temperatures. This test is only useful for failure mechanisms which are accelerated by temperature alone.

Test:	High-Temperature Storage
Test Conditions:	+150°C ambient temperature, unbiased, 1000 hours
Failure Criteria:	Must meet data sheet specifications
Results:	See Table 12

Statistical Process Control

Reliability testing offers little value if the manufacturing process varies widely. A standard assumption, which is often false, is that test samples pulled from production will be representative of the total population. The significance of sample variation can be reduced by increasing the sample size, but unless a process is "in control," variations will negatively affect quality and reliability. Under such conditions, reliability testing may disclose higher than desired failure rates, or widely varying test results.

Maxim monitors the stability of critical process parameters through the use of computerized Statistical Process Control (SPC). This provides our engineers with immediate feedback on process trends and shifts. Using this information, production processes can be maintained to tight tolerances, allowing us to provide the highest possible quality on a continuous basis.

In addition to the use of SPC for controlling process variation, Maxim uses Design of Experiments methodology to optimize process targeting and increase the "robustness" of each process.

Infant Mortality Evaluation

Maxim evaluates the infant mortality of all processes on an ongoing basis. Through infant mortality analysis, we can identify the common defects for each process. Once identified, corrective action can be taken to correct process related defects and improve overall reliability. Table 3 summarizes infant mortality data taken over an extended period of time.

TABLE 3: INFANT MORTALITY EVALUATION RESULTS

PRODUCT	LOT	BI TEMP	SS	FAIL	PPM	ANALYSIS
SH3 PROCESS*						
155-0289-02	LE10XXX	145	95	0	0	
	L501XXX	145	762	0	0	
	L502XXX	145	963	0	0	
	M41XXXX	145	1362	0	0	
	L503XXX	145	1310	0	0	
	L504XXX	145	1694	0	0	
155-0290-02	BE100XX	145	104	0	0	
	M41XXXX	145	671	0	0	
	L501XXX	145	566	2	3534	1 metal defect, 1 marginal trim
	L502XXX	145	719	0	0	
	L503XXX	145	767	0	0	
	L504XXX	145	220	0	0	
155-0371-02 M653 die	M502XXX	150	92	0	0	
	M503XXX	150	495	0	0	
	M504XXX	150	1054	0	0	
	M505XXX	150	481	0	0	
	M506XXX	150	324	0	0	
	M507XXX	150	126	0	0	
	M508XXX	150	569	0	0	
	M509XXX	150	194	0	0	
	M510XXX	150	404	0	0	
	M511XXX	150	186	0	0	
	M512XXX	150	303	0	0	
	M513XXX	150	403	0	0	
	M601XXX	150	580	0	0	
	M602XXX	150	489	0	0	
	M603XXX	150	192	0	0	
	M604XXX	150	201	0	0	
	X606XXX	150	380	1	2632	Mech. damage on die
Subtotal			16,706	3	180	
SHHV PROCESS*						
806-0004-22	M501XXX	150	1035	0	0	
	M503XXX	150	298	0	0	
	M506XXX	150	348	0	0	
	M510XXX	150	353	0	0	
	E10XXX	150	65	0	0	
155-0241-02	L504XXX	150	578	0	0	
	L506XXX	150	577	1	1733	Bond wire break
	L508XXX	150	666	0	0	
	510XXX	150	900	0	0	
	511XXX	150	272	0	0	
	512XXX	150	378	0	0	
	513XXX	150	771	0	0	
	601XXX	150	384	0	0	
	602XXX	150	3202	1	312	Bond wire break
	603XXX	150	487	0	0	
MAX445	X513XXX	150	587	0	0	
	L602XXX	150	98	0	0	
	X603XXX	150	118	0	0	
	M605XXX	150	209	0	0	
	X610XXX	150	76	0	0	
	Q609XXX	150	102	0	0	
	X612XXX	150	470	0	0	
	X701XXX	150	612	1	1634	Gain adjust out of spec
	X703XXX	150	192	0	0	
	X704XXX	150	484	0	0	
	X705XXX	150	487	0	0	
Subtotal			13,749	3	218	

** SH3 and SHHV processes are being phased out through use of GST-1 and GST-2 processes.*

TABLE 3: INFANT MORTALITY EVALUATION RESULTS (continued)

PRODUCT	LOT	BI TEMP	SS	FAIL	PPM	ANALYSIS
SHPi PROCESS						
806-0089-23	M502XXX	150	885	0	0	
	M503XXX	150	2669	0	0	
	M506XXX	150	1571	0	0	
	Q507056	150	384	0	0	
	M606XXX	150	71	0	0	
	X607XXX	150	911	0	0	
	X701XXX	150	876	1	1142	Supply current high
	X706XXX	150	1645	0	0	
806-0015-02 and MAX555	M501XXX	160	199	0	0	
	M503XXX	160	351	0	0	
	M504XXX	160	775	0	0	
	M505XXX	160	310	0	0	
	M506XXX	160	792	0	0	
	Q507XXX	160	200	0	0	
	M507XXX	160	1168	0	0	
	M508XXX	160	270	0	0	
	M509XXX	160	389	0	0	
	M511XXX	160	633	0	0	
	M605XXX	130	608	0	0	
	M607XXX	130	143	0	0	
	M609XXX	130	138	0	0	
	M610XXX	130	155	0	0	
	X701XXX	130	865	2	2260	Abs. gain error
	X706XXX	130	144	0	0	
155-0316-02	M503XXX	160	244	0	0	
	M504XXX	160	501	0	0	
	M505XXX	160	210	0	0	
	M506XXX	160	792	0	0	
	M507XXX	160	1168	0	0	
	M508XXX	160	270	0	0	
	M509XXX	160	181	0	0	
	M510XXX	160	292	0	0	
	M511XXX	160	197	0	0	
	M512XXX	160	396	0	0	
	M513XXX	130	598	0	0	
	M601XXX	130	153	0	0	
	M605XXX	130	465	0	0	
	M606XXX	130	320	0	0	
	M607XXX	130	277	1	3610	Continuity
	M608XXX	130	340	0	0	
	M609XXX	130	178	0	0	
	M610XXX	130	146	0	0	
	X701XXX	130	469	1	2132	Heatsink bond
	X704XXX	130	280	0	0	
	X706XXX	130	1021	0	0	
Subtotal			24,550	5	204	

TABLE 3: INFANT MORTALITY EVALUATION RESULTS (continued)

PRODUCT	LOT	BI TEMP	SS	FAIL	PPM	ANALYSIS
GST-1 PROCESS						
155-0371-02 (M726 die)	M502XXX	150	92	0	0	
	M503XXX	150	495	0	0	
	M504XXX	150	1054	3	2846	1 VOS shift, 1 M1-M1 short, 1 CE leak
	M505XXX	150	481	1	2079	Mechanical damage on die surface
	M506XXX	150	324	1	3086	Mechanical damage on die surface
	M507XXX	150	1126	0	0	
	M508XXX	150	569	0	0	
	M509XXX	150	194	0	0	
	M510XXX	150	404	0	0	
	M511XXX	150	186	0	0	
	M512XXX	150	303	0	0	
	M513XXX	150	403	0	0	
	M601XXX	150	580	0	0	
	M602XXX	150	489	0	0	
	M603XXX	150	192	0	0	
	M604XXX	150	201	0	0	
	X606XXX	150	380	0	0	
MAX3261	M605030	150	45	0	0	
	M608214	150	45	0	0	
MAX2101	M606XXX	150	65	0	0	
	M607XXX	150	80	0	0	
	Q511XXX	150	65	0	0	
	M701XXX	150	30	0	0	
	M702XXX	150	360	0	0	
	BHNAAQ	150	45	0	0	
Subtotal			8208	5	609	
GST-2 PROCESS						
MAX2452	M602050	150	45	0	0	
MAX3664	M606039	150	45	0	0	
MAX101	X605007	150	30	0	0	
MAX2430	M602092	150	40	0	0	
MAX3681	M611003	150	24	0	0	
8060300	CE10XXX	150	144	0	0	
8060300	Q504130	150	77	0	0	
Subtotal			415	0	0	
CPi						
MAX2402	M510XXX	150	45	0	0	
MAX3270	M509XXX	150	45	0	0	
MAX4278	BFXXX	150	135	0	0	
MAX41XX	BIXXX	135	676	0	0	
234XXXX	CE10XXX	150	138	0	0	
Subtotal			979	0	0	
CB2 PROCESS						
MAX4123	BJWACZ	135	80	0	0	
MAX4125	BJWBCZ	135	79	0	0	
MAX4131	BJWCCZ	135	80	0	0	
MAX3962	M611XXX	150	75	0	0	
Subtotal			314	0	0	
Total All Processes			**64,921**	**16**	**246**	

Field Failure Analysis

In addition to careful analysis of infant mortality failures, Maxim emphasizes analysis of returns from customers, to determine failure modes that can not be observed except through extensive long-term exposure in applications.

The information obtained from this analysis is also a useful tool in prioritizing quality improvement throughout the facility, from wafer fabrication through final test and shipping.

A recent summary of failure sources for customer returns is shown in the graph of Figure 5.

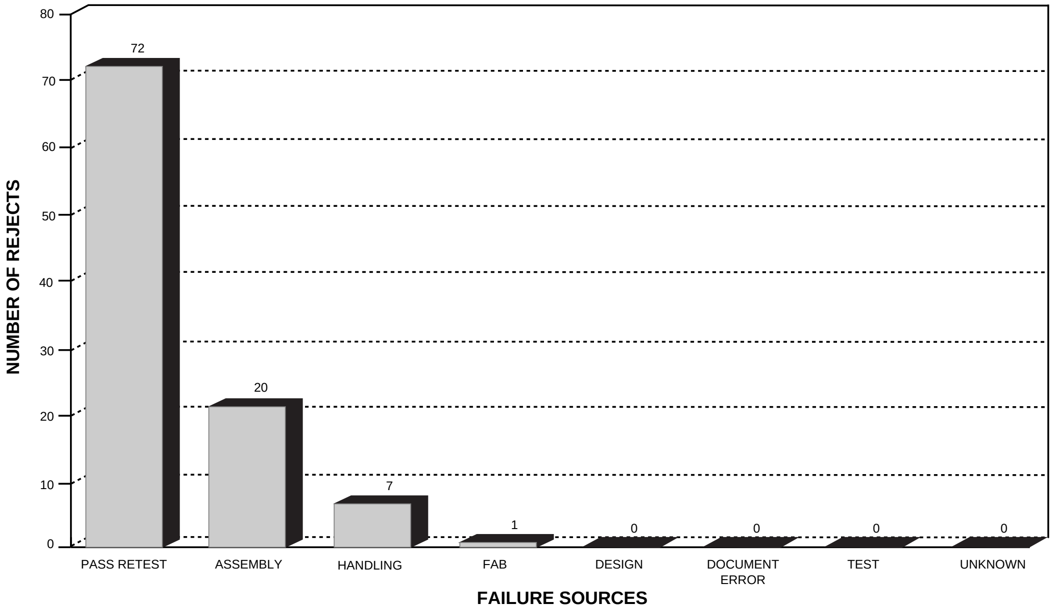

Figure 5: Failure Sources for Customer Returns

TABLE 4: LIFE TEST DATA—SHPi PROCESS

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES*		
				T1	T2	T3
155-0316-02	9513	68 TEQ	45	0	0	0
234-1115-20	9406	80 MQUAD	42	0	0	0
806-0003-20	9419	28 PLCC	45	0	0	0
806-0003-20	9430	28 PLCC	40	0	0	0
806-0015-22	9549	68 TEQ	10	0	0	0
806-0015-22	9551	68 TEQ	10	0	0	0
806-0015-22	9551	68 TEQ	45	0	0	0
806-0089-23	9450	28 CLCC	40	0	0	0
806-0089-23	9502	28 CLCC	40	0	0	0
806-0089-23	9502	28 CLCC	40	0	0	0
806-0189-31	NR	28 PLCC	77	0	0	0
806-0189-31	9447	28 PLCC	77	0	0	0
806-0189-31	9610	28 PLCC	45	0	0	0
806-0189-31	NR	28 PLCC	45	0	0	0
806-0189-31	9629	28 PLCC	45	0	0	0
806-0227-40	9444	48 SQFP	38	0	0	0
806-0227-40	9444	48 SQFP	39	0	0	0
806-0227-40	9406	48 SQFP	40	0	0	0
806-0227-40	9433	48 SQFP	40	0	0	0
806-0227-40	9648	48 SQFP	40	0	0	0
806-0232-22	9440	44 TEQ	30	0	0	0
806-0232-22	9448	44 TEQ	45	0	0	0
806-0232-22	9451	44 TEQ	45	0	0	0
806-0232-22	9502	44 PQUAD	30	0	0	0
806-0232-22	9506	44 PQUAD	30	0	0	0
806-0232-22	9522	44 PQUAD	30	0	0	0
806-0285-30	9519	36 QPF	45	0	0	0
806-0313-20	9444	44 MQFP	80	0	0	0
MAX3270	9508	44 MQFP	40	0	0	0
MAX4005	9442	8 SOIC	84	0	-	-
MAX555	NR	68 TEQ	72	0	0	0
MAX555CQK	9513	68 TEQ	44	0	0	0
MAX555CQK	9545	68 TEQ	44	0	0	0
MAX555CQK	9552	68 TEQ	45	0	0	0

TABLE 5: LIFE TEST DATA—GST-1 PROCESS

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES*		
				T1	T2	T3
155-0371-02	9447	84 MLC	45	0	0	0
155-0415-PQ	9519	160 PQUAD	10	0	0	0
155-0415-PQ	9519	160 PQUAD	10	0	0	0
155-0415-PQ	9526	160 PQUAD	10	0	0	0
806-0258-20	9410	32 PLCC	40	0	0	0
806-0286-20	9505	32 TQFP	45	0	0	0
806-0287-20	9504	24 SSOP	65	0	0	0
MAX100	NR	84 MLC	37	0	0	0
MAX100	NR	84 MLC	30	0	0	0
MAX2101	9411	100 MQFP	45	0	0	0
MAX2101	9434	100 MQFP	44	0	0	0
MAX2101	9443	100 MQFP	40	0	0	0
MAX2101	9502	100 MQFP	150	0	-	-
MAX2101	9452	100 PQUAD	45	0	0	0
MAX2101	9519	100 PQUAD	45	0	0	0
MAX2101	9519	100 PQUAD	20	0	0	0
MAX2101	9529	100 MQFP	45	0	0	0
MAX2101	9606	100 MQFP	30	0	0	0
MAX2101	9606	100 MQFP	30	0	0	0
MAX2101	9604	100 MQFP	20	0	0	0
MAX2101	9604	100 MQFP	20	0	0	0
MAX2101	NR	100 MQFP	180	0	-	-
MAX2101	9630	100 MQFP	15	0	0	0
MAX2101	9631	100 MQFP	15	0	0	0
MAX2101	NR	100 MQFP	135	0	-	-
MAX2101	9637	100 MQFP	45	0	-	-
MAX2101	9634	100 MQFP	45	0	0	0
MAX2101	9635	100 MQFP	45	0	0	0
MAX2101	9635	100 MQFP	45	0	0	0
MAX2101	9536	100 MQFP	45	0	0	0
MAX2452	9528	16 SOIC	45	0	-	-
MAX3260	9426	20 PDIP	60	0	-	-
MAX3261	9437	32 TQFP	45	0	0	0
MAX3261	NR	32 TQFP	41	0	0	0
MAX3261	9649	32 TQFP	44	0	0	0
MAX3261	9650	32 TQFP	44	0	0	0
MAX3262	9610	24 SSOP	45	0	-	-

** T1 = 168 hours, T2 = 500 hours, T3 = 1000 hours.*

TABLE 6: LIFE TEST DATA—GST-2 PROCESS

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES*		
				T1	T2	T3
806-0300-20	9440	20 PDIP	77	0	0	0
806-0300-20	NR	20 PDIP	77	0	0	0
806-0300-20	9503	20 PDIP	77	0	0	0
MAX101A	9605	84 MLC	30	0	0	0
MAX2430	A092	16 SOIC	38	0	0	0
MAX2452	9534	16 SOIC	45	0	0	0
MAX2602	9649	8 PSOP	45	0	0	0
MAX3664	9553	8 SOIC	45	0	0	0
MAX3681	9619	24 SSOP	30	0	0	0

TABLE 7: LIFE TEST DATA—CPi PROCESS

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES*		
				T1	T2	T3
234-1504-20	NR	44 PLCC	46	0	0	0
234-1504-20	NR	44 PLCC	46	0	0	0
234-1504-20	NR	28 QSOP	46	0	0	0
MAX2402CAP	9513	20 SSOP	45	0	0	0

TABLE 8: LIFE TEST DATA—CB2 PROCESS

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES*		
				T1	T2	T3
MAX3962	9627	28 QSOP	15	0	0	0
MAX3962	9628	28 QSOP	15	0	0	0
MAX3962	9623	28 QSOP	45	0	0	0

TABLE 9: 85/85 (THB) TEST DATA

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES*			NOTES
				T1	T2	T3	
155-0316-02	9513	68 TEQ	45	0	0	0	
155-0371-02	9447	84 MLC	18	0	0	0	
155-0415-PQ	9519	160 PQUAD	10	0	0	0	
155-0415-PQ	9519	160 PQUAD	10	0	0	0	
155-0415-PQ	9526	160 PQUAD	10	0	0	0	
234-1115-20	9406	80 MQUAD	36	0	0	0	
234-1504-20	NR	44 PLCC	44	0	0	0	
234-1504-20	NR	44 PLCC	44	0	0	0	
234-1504-20	NR	44 PLCC	44	1	1	0	Ball bond failure (2)
806-0003-20	9419	28 PLCC	45	0	0	1	Ball bond failure
806-0003-20	9430	28 PLCC	40	0	0	0	
806-0004-22	9426	24 PPDIP	45	0	0	5	Ni corrosion
806-0004-22	9437	24 PPDIP	45	0	0	0	
806-0004-22	9081	24 PPDIP	45	0	0	0	
806-0004-22	9511	24 PPDIP	45	0	0	0	
806-0015-20	9549	68 TEQ	10	0	0	0	
806-0015-20	9551	68 TEQ	10	0	0	0	
806-0089-23	9450	28 CLCC	40	0	0	0	
806-0089-23	9502	28 CLCC	40	0	0	0	
806-0089-23	9502	28 CLCC	40	0	0	0	
806-0189-31	NR	28 PLCC	45	0	0	0	
806-0189-31	9447	28 PLCC	45	0	0	0	
806-0189-31	NR	28 PLCC	45	0	0	0	
806-0189-31	9610	28 TEQ	20	0	0	0	
806-0189-31	9629	28 TEQ	45	0	1	0	Ball bond failure
806-0227-40	9406	48 SQFP	25	0	0	0	
806-0227-40	9433	48 SQFP	25	0	0	0	
806-0227-40	9444	48 SQFP	38	0	0	0	
806-0227-40	9444	48 SQFP	39	0	0	0	
806-0227-40	9648	48 SQFP	38	0	0	0	
806-0232-22	9448	48 TEQ	45	0	0	0	
806-0232-22	9451	44 TEQ	45	0	0	0	
806-0232-22	9502	44 PQUAD	30	0	0	0	
806-0232-22	9506	44 PQUAD	24	0	0	0	
806-0232-22	9522	44 PQUAD	30	0	0	0	
806-0258-20	9410	32 PLCC	25	0	0	0	
806-0286-20	9505	32 TQFP	38	0	0	0	
806-0300-20	9440	20 PDIP	75	0	0	0	
806-0300-20	9445	20 PDIP	75	0	0	0	
806-0300-20	9503	20 PDIP	45	0	0	0	
MAX100	NR	84 MLC	16	0	0	0	
MAX100	NR	84 MLC	29	0	0	0	
MAX445	9616	24 PPDIP	32	0	0	1	Ball bond failure
MAX555	9502	68 TEQ	80	0	0	0	
MAX555	9513	68 TEQ	45	0	0	0	
MAX555	9552	68 TEQ	45	0	0	0	
MAX2101	9434	100 MQFP	35	0	0	0	
MAX2101	9411	100 MQFP	45	0	0	0	

* T1 = 168 hours, T2 = 500 hours, T3 = 1000 hours.

TABLE 9: 85/85 (THB) TEST DATA (continued)

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES*			NOTES
				T1	T2	T3	
MAX2101	9443	100 MQFP	45	0	0	0	
MAX2101	9452	100 PQUAD	45	0	0	0	
MAX2101	9519	100 PQUAD	30	0	0	0	
MAX2101	9519	100 PQUAD	20	0	0	0	
MAX2101	9604	100 MQFP	20	0	0	0	
MAX2101	9604	100 MQFP	20	0	0	0	
MAX2101	9630	100 MQFP	10	0	0	0	
MAX2101	9631	100 MQFP	10	0	0	0	
MAX2101	9634	100 MQFP	45	0	0	0	
MAX2101	9635	100 MQFP	45	0	0	0	
MAX2101	9635	100 MQFP	45	0	0	0	
MAX2101	9536	100 MQFP	42	0	0	0	
MAX2452	9534	16 SOIC	36	0	0	0	
MAX3261	9437	32 TQFP	44	0	0	0	
MAX3261	9649	32 TQFP	40	0	0	0	
MAX3262	9610	24 SSOP	30	0	0	0	
MAX3664	9553	8 SOIC	45	0	0	0	
MAX3681	9619	24 SSOP	24	0	0	0	
MAX3962	9623	28 QSOP	45	0	0	0	
MAX3962	9627	28 QSOP	30	0	0	0	
MAX3962	9628	28 QSOP	30	0	0	0	

TABLE 10: PRESSURE POT TEST DATA (+121°C, 15 PSI, 100% RH)

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES @ 168 HOURS	NOTES
155-0371-02	9447	84 MLC	15	0	
155-0415-PQ	9519	160 PQUAD	15	0	
155-0415-PQ	9519	160 PQUAD	15	0	
155-0415-PQ	9526	160 PQUAD	20	0	
234-1115-20	9406	80 MQUAD	44	0	
234-1504-20	NR	44 PLCC	45	0	
234-1504-20	NR	44 PLCC	45	0	
234-1504-20	NR	44 PLCC	45	0	
806-0003-20	9419	28 PLCC	45	2	Ball bond failure
806-0003-20	9430	28 PLCC	40	0	
806-0004-20	9426	24 PPDIP	45	0	
806-0004-22	9437	24 PPDIP	45	0	
806-0004-22	9081	24 PPDIP	45	1	Ball bond failure
806-0004-22	9515	24 PPDIP	24	1	Ball bond failure
806-0015-20	9549	68 TEQ	20	0	
806-0015-21	9517	68 TEQ	20	0	
806-0015-22	9551	68 TEQ	20	0	
806-0089-23	9450	28 CLCC	45	0	
806-0089-23	9502	28 CLCC	45	0	
806-0089-23	9502	28 CLCC	45	0	
806-0189-31	9629	28 TEQ	30	0	
806-0227-40	9406	48 SQFP	15	0	
806-0227-40	9433	48 SQFP	25	0	
806-0227-40	9444	48 SQFP	45	0	
806-0227-40	9444	48 SQFP	45	0	
806-0227-40	9648	48 SQFP	45	0	
806-0227-40	9648	48 SQFP	45	0	
806-0232-22	9440	44 TEQ	45	0	
806-0232-22	9451	44 TEQ	30	0	
806-0232-22	9448	44 TEQ	10	0	
806-0232-22	9502	44 PQUAD	45	0	
806-0232-22	9506	44 PQUAD	20	0	
806-0232-22	9522	44 PQUAD	20	0	
806-0258-20	9410	32 PLCC	15	0	
806-0300-20	9440	20 PDIP	45	0	
806-0300-20	9445	20 PDIP	45	0	
806-0300-20	9503	20 PDIP	45	0	
MAX100	NR	84 MLC	15	0	
MAX2101	9427	100 MQFP	45	0	
MAX2101	9434	100 MQFP	45	0	

* T1 = 168 hours, T2 = 500 hours, T3 = 1000 hours.

TABLE 10: PRESSURE POT TEST DATA (+121°C, 15 psi, 100% RH) (continued)

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES @ 168 HOURS	NOTES
MAX2101	9443	100 MQFP	40	0	
MAX2101	9452	100 PQUAD	45	0	
MAX2101	9519	100 PQUAD	40	2	Ball bond failure
MAX2101	9519	100 PQUAD	15	0	
MAX2101	9603	100 PQUAD	15	0	
MAX2101	9604	100 MQFP	15	0	
MAX2101	9604	100 MQFP	15	0	
MAX2101	9634	100 MQFP	40	0	
MAX2101	9635	100 MQFP	40	0	
MAX2101	9635	100 MQFP	40	0	
MAX2101	9701	100 MQFP	45	0	
MAX2101	9702	100 MQFP	45	0	
MAX2452	9534	16 SOIC	40	0	
MAX3261	9505	32 TQFP	45	0	
MAX3261	9437	32 TQFP	30	0	
MAX3261	9649	32 TQFP	45	0	
MAX3261	9650	32 TQFP	45	0	
MAX3262	9610	24 SSOP	8	0	
MAX3664	9553	8 SOIC	45	0	
MAX3681	9619	24 SSOP	45	0	
MAX3962	9623	28 QSOP	45	0	
MAX3962	9627	28 QSOP	40	0	
MAX3962	9628	28 QSOP	40	0	
MAX555	9084	68 TEQ	35	7	LWT shift**
MAX555	9502	68 TEQ	20	1	LWT shift**
MAX555	9502	68 TEQ	20	0	

TABLE 11: TEMPERATURE-CYCLING TEST DATA (-55°C to +125°C, 1000 cycles)

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES†			NOTES
				T1	T2	T3	
155-0371-02	9447	84 MLC	20	0	0	0	
155-0415-PQ	9519	160 PQUAD	20	0	0	0	
155-0415-PQ	9519	160 PQUAD	20	0	0	0	
234-1115-20	9406	80 MQUAD	43	0	0	0	
234-1504-20	NR	44 PLCC	45	0	0	0	
234-1504-20	NR	44 PLCC	45	0	0	0	
234-1504-20	NR	44 PLCC	45	0	0	0	
806-0003-20	9419	28 PLCC	45	0	0	0	
806-0003-20	9430	28 PLCC	45	0	0	0	
806-0004-22	9426	24 PPDIP	45	0	0	0	
806-0004-22	9437	24 PPDIP	45	0	0	0	
806-0004-22	9515	24 PPDIP	30	0	0	0	
806-0015-22	9549	68 TEQ	25	0	0	0	
806-0015-22	9517	68 TEQ	30	0	0	0	
806-0015-22	9551	68 TEQ	25	0	0	0	
806-0089-23	9450	28 CLCC	45	0	0	0	
806-0089-23	9502	28 CLCC	45	0	0	0	
806-0089-23	9502	28 CLCC	45	0	0	0	
806-0227-40	9406	48 SQFP	25	0	–	–	100 cycles
806-0227-40	9433	48 SQFP	30	0	0	0	
806-0227-40	9444	48 SQFP	45	0	0	0	
806-0227-40	9444	48 SQFP	45	0	0	0	
806-0232-22	9440	44 TEQ	45	0	0	0	
806-0232-22	9448	44 TEQ	45	0	0	0	
806-0232-22	9451	44 TEQ	45	0	0	0	
806-0232-22	9502	44 PQUAD	45	0	0	0	
806-0232-22	9506	44 PQUAD	30	0	0	0	
806-0232-22	9522	44 PQUAD	30	0	0	0	
806-0258-20	9410	32 PLCC	110	0	–	–	
806-0285-30	9519	36 QFP	15	0	–	–	
806-0300-20	9440	20 PDIP	45	0	0	0	
806-0300-20	9445	20 PDIP	45	0	0	0	
806-0300-20	9503	20 PDIP	36	0	0	0	

†T1 = 200 cycles, T2 = 500 cycles, T3 = 1000 cycles.

*** Laser Wafer Trimmed precision resistor shift. Burn-in implemented as screen for product.*

TABLE 11: TEMPERATURE-CYCLING TEST DATA (-55°C to +125°C, 1000 cycles) (continued)

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES† T1	T2	T3	NOTES
MAX100	NR	84 MLC	15	0	0	0	
MAX100	NR	84 MLC	15	0	0	0	
MAX2101	9427	100 MQFP	45	0	0	0	
MAX2101	9434	100 MQFP	41	0	0	0	
MAX2101	9443	100 MQFP	40	0	0	0	
MAX2101	9452	100 PQUAD	44	0	0	0	
MAX2101	9519	100 PQUAD	45	0	0	0	
MAX2101	9519	100 PQUAD	20	0	0	0	
MAX2101	9604	100 MQFP	20	0	0	0	
MAX2101	9604	100 MQFP	20	0	0	0	
MAX2101	9606	100 MQFP	20	0	0	0	
MAX2101	9634	100 MQFP	45	0	0	0	
MAX2101	9635	100 MQFP	45	0	0	0	
MAX2101	9635	100 MQFP	45	0	0	0	
MAX2452	9534	16 SOIC	45	0	0	0	
MAX3261	9437	32 TQFP	45	0	0	0	
MAX3261	9505	32 TQFP	45	0	0	0	
MAX3261	9705	32 TQFP	45	0	0	0	
MAX3664	9553	8 SOIC	40	0	0	0	
MAX3681	9619	24 SSOP	40	0	0	0	
MAX3962	9623	28 QSOP	45	0	0	0	
MAX3962	9627	28 QSOP	45	0	0	0	
MAX3962	9628	28 QSOP	45	0	0	0	
MAX555	9425	68 TEQ	45	0	0	0	
MAX555	9545	68 TEQ	30	0	0	0	

TABLE 12: HIGH-TEMPERATURE STORAGE TEST RESULTS

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES* T1	T2	T3	NOTES
155-0371-02	9447	84 MLC	15	0	0	0	
155-0415-PQ	9519	160 PQUAD	20	0	0	0	
155-0415-PQ	9519	160 PQUAD	20	0	0	0	
155-0415-PQ	9526	160 PQUAD	20	0	0	0	
234-1115-20	9406	80 MQUAD	45	0	0	0	
234-1504-20	NR	44 PLCC	45	0	0	0	
234-1504-20	NR	44 PLCC	45	0	0	0	
234-1504-20	NR	44 PLCC	45	0	0	0	
806-0003-20	9419	28 PLCC	45	0	0	0	
806-0003-20	9430	28 PLCC	30	0	0	0	
806-0004-22	9426	24 PPDIP	45	0	0	0	
806-0004-22	9437	24 PPDIP	45	0	0	0	
806-0004-22	9081	24 PPDIP	45	0	0	0	
806-0004-22	9515	24 PPDIP	30	0	0	0	
806-0015-21	9549	68 TEQ	20	0	0	0	
806-0015-21	9517	68 TEQ	30	0	0	0	
806-0015-21	9551	68 TEQ	20	0	0	0	
806-0089-23	9450	28 CLCC	30	0	0	0	
806-0089-23	9502	28 CLCC	30	0	0	0	
806-0089-23	9502	28 CLCC	30	0	0	0	
806-0189-31	9629	28 TEQ	30	0	0	1	ESD
806-0227-40	9406	48 SQFP	40	0	0	0	
806-0227-40	9433	48 SQFP	25	0	0	0	
806-0227-40	9444	48 SQFP	45	0	0	0	
806-0227-40	9444	48 SQFP	45	0	0	0	
806-0227-40	9648	48 SQFP	28	0	0	0	
806-0227-40	9648	48 SQFP	40	0	0	0	
806-0232-22	9440	44 TEQ	45	0	0	0	
806-0232-22	9451	44 TEQ	30	0	0	0	
806-0232-22	9448	44 TEQ	40	0	0	0	
806-0232-22	9502	44 PQUAD	38	0	0	0	
806-0232-22	9506	44 PQUAD	40	0	0	0	
806-0232-22	9522	44 PQUAD	30	0	0	0	

† T1 = 200 cycles, T2 = 500 cycles, T3 = 1000 cycles.
* T1 = 168 hours, T2 = 500 hours, T3 = 1000 hours.

TABLE 12: HIGH-TEMPERATURE STORAGE TEST RESULTS (continued)

DEVICE TYPE	DATE CODE	PACKAGE	SAMPLE SIZE	FAILURES*			NOTES
				T1	T2	T3	
806-0300-20	9440	20 PDIP	45	0	0	0	
806-0300-20	9445	20 PDIP	45	0	0	0	
806-0300-20	9503	20 PDIP	45	0	0	0	
MAX2101	9427	100 MQFP	45	0	0	0	
MAX2101	9434	100 MQFP	45	0	0	0	
MAX2101	9443	100 MQFP	30	0	0	0	
MAX2101	9452	100 PQUAD	40	0	0	0	
MAX2101	9519	100 PQUAD	45	0	0	0	
MAX2101	9519	100 PQUAD	20	0	0	0	
MAX2101	9604	100 MQFP	20	0	0	0	
MAX2101	9604	100 MQFP	20	0	0	0	
MAX2101	9634	100 MQFP	40	0	0	0	
MAX2101	9635	100 MQFP	40	0	0	0	
MAX2101	9635	100 MQFP	40	0	0	0	
MAX2101	9701	100 MQFP	30	0	0	0	
MAX2101	9702	100 MQFP	45	0	0	0	
MAX2452	9534	16 SOIC	45	0	0	0	
MAX3261	9505	32 TQFP	45	0	0	0	
MAX3261	9437	32 TQFP	45	0	0	0	
MAX3261	9649	32 TQFP	45	0	0	0	
MAX3261	9650	32 TQFP	40	0	0	0	
MAX3664	9553	8 SOIC	45	0	0	0	
MAX3681	9619	24 SSOP	45	0	0	0	
MAX3962	9623	28 QSOP	45	0	0	0	
MAX3962	9627	28 QSOP	45	0	0	0	
MAX3962	9628	28 QSOP	45	0	0	0	
MAX555	9407	68 TEQ	28	0	8	8	LWT shift**
MAX555	9502	68 TEQ	38	0	0	0	
MAX555	9502	68 TEQ	30	0	0	0	
MAX555	9513	68 TEQ	45	0	0	0	
MAX555	9552	68 TEQ	20	0	0	0	

* T1 = 168 hours, T2 = 500 hours, T3 = 1000 hours.

** *Laser Wafer Trimmed precision resistor shift. Burn-in implemented as screen for product.*

Appendices

Appendix 1: Determining Acceleration Factor

Definition of Terms

An acceleration factor is a constant used in reliability prediction formulas that expresses the effect of temperature on a device's failure rate over time. Generally, semiconductor devices degrade faster as temperature increases. For that reason, operating devices at elevated temperatures allows long-term testing to be accomplished at an accelerated rate, shortening the overall time needed to verify good reliability failure rates. In simple terms, a statement such as, "The failure rate of these devices operating at +150°C is 369 times greater than the failure rate at +75°C," implies an acceleration factor of 369.

The acceleration factor typically used throughout the semiconductor industry is derived using the Arrhenius equation:

$$\text{Acceleration Factor (AF)} = e^{\frac{E_a}{K}\left(\frac{1}{T1} - \frac{1}{T2}\right)}$$

Where: E_a = activation energy (electron volts)
k = Boltzmann's constant
T1 = derating temperature (Kelvin)
T2 = acceleration temperature (Kelvin)

How to Use the Arrhenius Equation

The first step in calculating an acceleration factor is to determine the activation energy for the predominant failure mechanism. This can be done quantitatively by observing the mechanism of failure and selecting an activation energy from numerous existing tables. For example, intermetallic growth is defined as an activation energy of 1.0eV, oxide pinholes is 0.7eV, etc.

To qualitatively define the activation energy, one must first derive the value through experimentation. Failure analysis techniques are employed to determine failure mechanisms for devices that have failed as a result of high-temperature stress testing. Once the primary mechanism has been identified, additional Life Tests at various elevated temperatures may be performed, and continue until some percentage of the population fails for that mechanism. From that information, a calculation can be created which defines the activation energy, in electron volts.

Assuming two groups of samples have been run at two different temperatures, the number of failures from both groups is totaled:

Group 1: 9822 failures after 100 hrs operation at +150°C
Group 2: 1 failure after 100 hours operation at +25°C

The acceleration factor for the failure mechanism between the two temperatures is 9822 / 1, or 9822.

The Arrhenius equation can be rewritten as follows:

$$AF = 9822 = e^{\frac{E_a}{K}\left(\frac{1}{T1} - \frac{1}{T2}\right)}$$

Where: E_a = unknown
k = 8.63×10^{-5}eV / °K
T1 = +25°C + +273°C (298°K)
T2 = +150°C + +273°C (423°K)

Solving the equation for the activation energy results in approximately 0.8eV.

Assuming the activation energy found represents the dominant failure mechanism of the device under consideration, it may then be used to determine the acceleration factor between any two temperatures. For example, if the test temperature is +150°C and the application (derating) temperature is +70°C, the calculation for acceleration factor, with 0.8eV activation energy, is 165.

Appendix 2: Determining Failure Rate

Definition of Terms

The Mean Time Between Failures (MTBF) is the average time it takes for a failure to occur. For example, assume a company tests 100 units for 1000 hours. The total device-hours accrued would be 100 x 1000, or 100,000 device-hours. Now assume two units were found to be failures. Roughly, it could be said the MTBF would equal:

$$\text{MTBF} = \frac{\text{Total device-hours}}{\text{Total no. of failures}} = \frac{100{,}000}{2} = 50{,}000$$

The failure rate is equal to the reciprocal of the MTBF, or:

$$\text{Failure Rate} = \frac{1}{\text{MTBF}} = \frac{1}{50{,}000} = 0.00002$$

Multiplying this number by 1 x 10^5 yields the failure rate, in terms of percent per 1000 hours. For our example, the failure rate is 0.2%.

A common reliability term also used to express the failure rate is Failures-in-Time, or FIT. This is the number of failures per one billion device-hours, and is obtained by dividing the failure rate by 10^{-9}. Continuing with the example above, the failure rate in FITs is:

$$0.00002 / 10^{-9} = 20{,}000$$

The FIT rate is, therefore, the number of units predicted to fail in one billion (10^9) device-hours at a specific temperature.

Calculating Failure Rates and FITs

The failure rate can be expressed in terms of the following four variables:

A = number of failures observed
B = number of hours the test was run
C = number of samples used
D = temperature acceleration factor

Assume the following is true:

A = 2
B = 1000 hours (HTOL)
C = 824
D = temperature acceleration factor

Where:

$$D = e^{\frac{0.8}{8.63 \text{ x } 10^{-5}} \times \left(\frac{1}{T1} - \frac{1}{T2}\right)}$$

$$= e^{\left[9269.98 \text{ x } \left(\frac{1}{298} - \frac{1}{423}\right)\right]}$$

$$= 9822$$

Substituting into the equation for failure rate:

FR = 1 / MTBF
= 1 / [(B x C x D) / 2]
= 1 / [(1000 x 824 x 9822) / 2]
= 2.471 x 10^{-10}

Converting to FITs by multiplying by 10^9, the failure rate is 0.247 FITs.

Including Statistical Effects in the FIT Calculation

Because a small random sample is being chosen from each lot, the statistical effects are significant enough to mention. With most published failure-rate figures, there is an associated confidence level number. This number expresses the confidence level that the actual failure rate of the lot will be equal to, or lower than, the predicted failure rate.

The failure-rate calculation, including a confidence level, is determined as follows:

FR = x^2 / 2DH

Where:

x^2 = the Chi square value
2DH = 2 times the total device hours
= 2 x (B x C x D)

The Chi square value is based on a particular type of statistical distribution. However, all that is required to arrive at this value is knowing the number of failures. In this example there were two failures and, using a Chi square distribution table, a value of 6.21 is found. Thus, with a 60% confidence level, the failure rate for our example is:

FR = 6.21 / 2 x 8.093 x 10^9
= 3.836 x 10^{-10}
= 0.383 FITs