

SCOPE: QUAD, CMOS, 8-BIT D/A CONVERTER

<u>Device Type</u>	<u>Generic Number</u>	<u>Circuit Function</u>
01	MX7226T(x)/883B	DAC with 2 LSB

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
Maxim SMD			
Q R	GDIP1-T20 or CDIP2-T20	20 LEAD CERDIP	J20
E 2	CQCC1-N20	20 LCC	L20

Absolute Maximum Ratings: 1/

V _{DD} to AGND	-0.3V dc, +17V
V _{DD} to DGND	-0.3V dc, +17V
V _{DD} to V _{SS}	-0.3V dc to +24V
AGND to DGND	-0.3V dc to V _{DD}
Digital Input Voltage to DGND	-0.3V dc to V _{DD}
V _{REF} to AGND	-0.3V dc to V _{DD}
V _{OUT} to AGND 2/.....	V _{SS} , V _{DD}

Lead Temperature (soldering, 10 seconds)	+300°C
Storage Temperature	-65°C to +150°C

Continuous Power Dissipation	T _A =+70°C
20 pin CERDIP(derate 11.1mW/°C above +70°C)	889mW
20 pin LCC(derate 9.1mW/°C above +70°C)	727mW
Junction Temperature T _J	+150°C
Thermal Resistance, Junction to Case, θ_{JC}	
20 pin CERDIP.....	40°C/W
20 pin LCC	20°C/W
Thermal Resistance, Junction to Ambient, θ_{JA} :	
20 pin CERDIP.....	90°C/W
20 pin LCC	110°C/W

Recommended Operating Conditions

Ambient Operating Range (T _A)	-55°C to +125°C
Power Supply Range (V _{DD})	+11.4V dc to +16.5V dc
Input Reference Voltages:	
Dual Supply Operation	+2.0V dc to V _{DD} -4V dc
Single Supply Operation	+10.0V dc

NOTE 1: Unless otherwise specified all voltages are referenced to ground.

NOTE 2: Outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typical short circuit current to AGND is 60mA.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS	Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C ≤ T _A ≤ +125 °C 3/ Unless otherwise specified					
POWER SUPPLIES							
Positive Supply Current from V _{DD}	I _{DD}	V _{IN} =V _{INL} or V _{INH} , Outputs Unloaded	1,2,3	All		13	mA
Negative Supply Current from V _{SS}	I _{SS}	V _{IN} =V _{INL} or V _{INH} , Outputs Unloaded	1,2,3	All		11	mA
REFERENCE INPUT							
Reference Voltage	V _{REF}				2	V _{DD} -4	V
Reference Input Resistance	R _{IN}		1,2,3	All	2		kΩ
Reference Input Capacitance	C _{IN}	DAC loaded with all 1s	4	All		300	pF
STATIC PERFORMANCE							
Total Unadjusted Error	ET	V _{DD} =+15V±5%, V _{REF} =+10V	1,2,3	All	-2.0	2.0	LSB
Relative Accuracy	RA		1,2,3	All	-1.0	1.0	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic	1,2,3	All	-1.0	1.0	LSB
Full-Scale Error	AE		1,2,3	All	-1.5	1.5	LSB
Zero-Code Error			1,2,3	All	-30	30	mV
DIGITAL INPUTS							
Input High Voltage	V _{INH}		1,2,3	All	2.4		V
Input Low Voltage	V _{INL}		1,2,3	All		0.8	V
Input Leakage Current	I _{ILKG}	V _{IN} =0V or V _{DD}	1,2,3	All	-1.0	1.0	μA
Functional Tests		Verify the Truth Table	7	All			
DYNAMIC PERFORMANCE							
Voltage Output Slew Rate	T _{SR}	NOTE 4	4,5,6	All	2.5		V/μs
Voltage Output Settling Time (positive full scale change) NOTE 4	T _{SL}	Settling time to ±0.5LSB, REF=+10V	4,5,6	All		5	μs
Voltage Output Settling Time (negative full scale change) NOTE 4	T _{SL}	Settling time to ±0.5LSB, REF=+10V	4,5,6	All		7	μs
Load Resistance	R _L MIN	V _{OUT} =+10V	4	All	2		kΩ
SWITCHING CHARACTERISTICS							
Write Pulse Width, t1	t _{WR}		9 10,11	All	150 250		ns
Address to Write-Setup Time, t2	t _{AS}		9	All	0		ns
Address to Write-Hold Time, t3	t _{AH}		9	All	10		ns
Data Valid to Write Set-up Time, t4	t _{DS}		9 10,11	All	90 100		ns
Data Valid to Write Hold Time, t5	t _{DH}		9,10,11	All	10		ns

TEST	Symbol	CONDITIONS		Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C <=T _A <= +125°C 5/ Unless otherwise specified						
POWER SUPPLIES								
Positive Supply Current from V _{DD}	I _{DD}	V _{IN} =V _{INL} or V _{INH} , Outputs Unloaded	1,2,3	All		13		mA
REFERENCE INPUT								
Load Resistance	R _{LMIN}	V _{OUT} =10V	4	All	2			kΩ
Reference Input Resistance	R _{IN}		1,2,3	All	2			kΩ
Reference Input Capacitance	C _{IN}	DAC loaded with all 1s	4	All		300		pF
STATIC PERFORMANCE								
Total Unadjusted Error	E _T		1,2,3	All	-2.0	2.0		LSB
Differential Nonlinearity	DNL	Guaranteed monotonic	1,2,3	All	-1.0	1.0		LSB
DIGITAL INPUTS								
Input High Voltage	V _{INH}		1,2,3	All	2.4			V
Input Low Voltage	V _{INL}		1,2,3	All		0.8		V
Input Leakage Current	I _{ILKG}	V _{IN} =0V or V _{DD} ,	1,2,3	All	-1.0	1.0		μA
Functional Tests		Verify the Truth Table	7	All				
DYNAMIC PERFORMANCE								
Voltage Output Slew Rate	T _{SR}	NOTE 4	4,5,6	All	2.5			V/μs
Voltage Output Settling Time (positive full scale change) NOTE 4	T _{SL}	Settling time to ±0.5LSB	4,5,6	All		5		μs
Voltage Output Settling Time (negative full scale change) NOTE 4	T _{SL}	Settling time to ±0.5LSB	4,5,6	All		20		μs
SWITCHING CHARACTERISTICS								
Write Pulse Width, t1	t _{WR}		9 10,11	All	150 250			ns
Address to Write-Setup Time, t2	t _{AS}		9	All	0			ns
Address to Write-Hold Time, t3	t _{AH}		9	All	10			ns
Data Valid to Write Set-up Time, t4	t _{DS}		9 10,11	All	90 100			ns
Data Valid to Write Hold Time, t5	t _{DH}		9,10,11	All	10			ns

NOTE 3: Dual-Supply operation, V_{DD}=+11.4V to +16.5, V_{SS}=-5V±10%, AGND=DGND=0V, VREF= +2V to (V_{DD}-4V), unless otherwise specified.

NOTE 4: Guaranteed if not tested to the limits specified.

NOTE 5: Single-supply operation, V_{DD}=+15V±5%, V_{SS}=AGND=DGND=0V, VREF=+10V unless otherwise specified.

TRUTH TABLE:

$\overline{\text{WR}}$	A1	A0	SELECTED INPUT REGISTER
H	X	X	No operation. Device not selected
L	L	L	DAC A transparent
↑	L	L	DAC A latched
L	L	H	DAC B transparent
↑	L	H	DAC B latched
L	H	L	DAC C transparent
↑	H	L	DAC C latched
L	H	H	DAC D transparent
↑	H	H	DAC D latched

L = Low State, H = High State, X = Don't care

TERMINAL CONNECTIONS:

Pin	J20/L20	Pin	J20/L20
1	V _{OUTB}	11	D3
2	V _{OUTA}	12	D2
3	V _{SS}	13	D1
4	VREF	14	D0(LSB)
5	AGND	15	$\overline{\text{WR}}$
6	DGND	16	A1
7	D7(MSB)	17	A0
8	D6	18	V _{DD}
9	D5	19	V _{OUTD}
10	D4	20	V _{OUTC}

	Package	ORDERING INFORMATION:	SMD Number
01	20 pin CERDIP	MX7226TQ/883B	5962-8780201RA
01	20 pin LCC	MX7226TE/883B	5962-87802012C

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
 1. Test condition A, B, C, D.
 2. TA = +125°C, minimum.
 3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 4**, 5, 6, 7, 9, 10***, 11***
Group C and D End-Point Electrical Parameters Method 5005	1

- * PDA applies to Subgroup 1 only.
- ** Subgroup 4, capacitance tests shall be tested at initial qualification and upon redesign. Sample size will be 116 units.
- *** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in Table 1.