

SCOPE: CMOS, TTL-COMPATIBLE ANALOG MULTIPLEXER

<u>Device Type</u>	<u>Generic Number</u>
01	DG528A(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
K	GDIP1-T18 or CDIP2-T18	18 LEAD CERDIP	J18

Absolute Maximum Ratings

Voltage Referenced to V⁻

V ⁺ to V ⁻	44V
V ⁺ to GND	25V
Digital Inputs, V _S , V _D	(-V) -2V to (V ⁺)+2V or 20mA, whichever occurs first
Current, Any terminal except S or D	30mA
Continuous Current, S or D	20mA
Peak Current S or D (Pulsed at 1ms, 10% duty cycle max)	40mA
Lead Temperature (soldering, 10 seconds)	+300°C
Storage Temperature	-65°C to +150°C
Continuous Power Dissipation	T _A =+70°C
18 lead CERDIP(derate 10.5mW/°C above +70°C)	842mW
Junction Temperature T _J	+150°C
Thermal Resistance, Junction to Case, Θ _{JC} :	
Case Outline 18 lead CERDIP.....	45°C/W
Thermal Resistance, Junction to Ambient, Θ _{JA} :	
Case Outline 18 lead CERDIP.....	95°C/W

Recommended Operating Conditions.

Ambient Operating Range (T _A)	-55°C to +125°C
Positive Supply Voltage (V ⁺)	+15V
Negative Supply Voltage (V ⁻)	-15V
V _{AL} (max)	0.8V
V _{AH} (min)	2.4V

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS

TEST	Symbol	CONDITIONS	Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C ≤ T _A ≤ +125°C $\frac{1}{\text{---}}$ V ₊ =+15V, V ₋ =-15V, $\frac{1}{\text{---}}$ RS=2.4V, GND=WR=0V, V _{AH} =2.4V, V _{AL} =0.8V Unless otherwise specified					
SWITCH							
Analog-Signal Range	V _{ANALOG}	V _S =±15V	1,2,3	All	-15	15	V
Drain-Source ON Resistance	r _{DS(ON)}	I _S = -200μA, V _D =±10V, V _{AL} =0.8V, V _{AH} =2.4V, Sequence each switch ON	1 2,3	All		400 500	Ω
Source OFF Leakage Current	I _{S(OFF)}	V _S =10mA, V _D =-10V, V _{EN} =0V	1 2,3	All	-1 -50	1 50	nA
Source OFF Leakage Current	I _{S(OFF)}	V _S =-10mA, V _D =10V, V _{EN} =0V	1 2,3	All	-1 -50	1 50	nA
Drain OFF Leakage Current	I _{D(OFF)}	V _S =±10mA, V _D =±10V, V _{EN} =0V	1 2,3	All	-10 -200	10 200	nA
Drain ON Leakage Current NOTE 2	I _{D(ON)}	V _D =V _S =±10V, V _{AL} =0.8V, V _{AH} =4.0V, V _{EN} =2.4V, Sequence each switch ON.	1 2,3	All	-10 -200	10 200	nA
INPUT							
Input Current/Voltage High	I _{AH}	V _{IN} = 2.4V	1 2,3	All	-10 -30		μA
		V _{IN} =15V	1 2,3	All		10 30	
Input Current/Voltage Low	I _{AL}	V _{EN} =0V, 2.4V; V _A =0V, $\frac{1}{\text{---}}$ $\frac{1}{\text{---}}$ V _A =WR=RS=0V	1 2,3	All	-10 -30		μA
SUPPLY							
Positive Supply Current	I ₊	V _{EN} =V _A =0V	1 2,3	All		2.5 4.0	mA
Negative Supply Current	I ₋	V _{EN} =V _A =0V	1 2,3	All	-1.5 -4.0		mA
Functional Tests		Testing sufficient to verify Truth Table	7,8				
DYNAMIC							
Transition Time	t _{TRANS}	Figure 1	9 10,11	All		1.0 1.5	μs
Enable and Write Turn ON Time	t _{ON} $\frac{1}{\text{---}}$ (EN, WR)	See Figures 2 and 3	9 10,11	All		1.0 1.5	μs
Enable and Write Turn OFF Time	t _{OFF} $\frac{1}{\text{---}}$ (EN, RS)	See Figures 2 and 3	9 10,11	All		1.0 1.5	μs

NOTE 1: Period of reset (RS) pulse must be at least 50μs during or after power ON.

NOTE 2: ID(ON) is leakage from driver into “ON” switch.

FIGURE 1: TRANSITION TIME TEST CIRCUIT: See Commercial Data Sheet

FIGURE 2: Enable t_{ON}/t_{OFF} Test Time Circuit: See Commercial Data Sheet

FIGURE 3: Write Turn-On Time Test Circuit: See Commercial Data Sheet

ORDERING INFORMATION:	SMD Number	Package Code
DG528AK/883B	5962-8768901VA	18 CDIP

TRUTH TABLE

TERMINAL CONNECTION

A2	A1	A0	EN	\overline{WR}	\overline{RS}	DG528A ON SWITCH	TERMINAL NUMBER	01 DG528A
X	X	X	X	↑	1	*		J18
X	X	X	X	X	0	**	1	\overline{WR}
X	X	X	0	0	1	None	2	A0
0	0	0	1	0	1	1	3	EN
0	0	1	1	0	1	2	4	V-
0	1	0	1	0	1	3	5	S1
0	1	1	1	0	1	4	6	S2
1	0	0	1	0	1	5	7	S3
1	0	1	1	0	1	6	8	S4
1	1	0	1	0	1	7	9	D
1	1	1	1	0	1	8	10	S8
							11	S7
							12	S6
							13	S5
							14	V+
							15	GND
							16	A2
							17	A1
							18	\overline{RS}

* LATCHING: Maintains previous switch conditions

** RESET: None (latches cleared)

NOTE: Logic "1": $V_{AH} \geq 2.4V$

Logic "0": $V_{AL} \geq 0.8V$

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
 1. Test condition A, B, C, D.
 2. TA = +125°C, minimum.
 3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 7, 8**, 9, 10, 11***
Group A Test Requirements Method 5005	1, 2, 3, 7, 8**, 9, 10, 11***
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroups 7 and 8 tests shall be sufficient to verify the truth tables.

*** Subgroups 10 and 11, if not tested shall be guaranteed to the limits of Table 1.